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Mitigation of Power Quality Problems Using Novel DSTATCOM Operating Under Stiff Source

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Abstract: ***Normally induction motors connected to a stiff source cannot be protected from voltage disturbances in a distribution system using a distribution static compensator (DSTATCOM). A normal DSTATCOM can operate either in Voltage Control Mode (VCM) or Current Control Mode (CCM). When an induction motor operated under stiff source may get faults either from voltage disturbances or current disturbances. To solve this, a new control algorithm is proposed to make as multifunctional i.e, operated in VCM under stiff source and CCM in normal operation. From this, a fast voltage regulation is achieved at the load terminal and protects induction machine drive system during voltage disturbances and current disturbances. In this paper major power quality faults i.e, sag is injected and compensated using multifunctional DSTATCOM. The complete project is carried out using MATLAB/SIMULINK.***

Keywords : stiff source, DSTATCOM, induction motor, sag, load angle.

I. Introduction

A distribution static compensator (DSTATCOM) is a shunt connected device, operate in different modes to diminish several power quality problems[i]. It injects harmonics and reactive components of load currents when operated in current control mode(CCM).In voltage control mode(VCM)**,** it protects sensitive loads from voltage disturbances such as sags, transients, swells or fluctuations by regulating load voltage at constant value. However, these two modes of operation cannot be achieved simultaneously.

Depends on source to load distance, a source is termed as stiff or nonstiff. If the distance is long, then source is termed as nonstiff, whereas if the distance is low, it is termed as stiff source and has negligible feeder impedance. For satisfactory performance, a source (stiff or nonstiff) always supply permissible range of voltage to load terminal. In this condition, CCM operation should be performed by DSTATCOM. Due to grid faults, the source voltage can change at any instant of time, in this situation VCM operation is required. This can be achieved indirectly by regulating the voltage across the feeder impedance through DSTATCOM. Due to negligible feeder impedance, if the load is connected to stiff source, voltage regulation at the load terminals cannot be achieved by DSTATCOM. This problem can be overcome in this present work, without effecting normal operation.

A new controlled DSTATCOM is used in this paper to regulate the voltage even under stiff source by connecting a suitable external inductor in series between source and load terminal. The point at which the external inductor and source are connected, it is termed as the point of common coupling (PCC). When DSTATCOM operate in VCM connected at load terminals[8], it regulates load voltage by indirectly regulating the voltage across external inductor. The proposed control is formulated as a function of desired source currents to obtain required reference load voltages. For a certain range of source voltages, currents drawn by the source was indirectly controlled from reference load voltages. During normal operation the new control makes source currents sinusoidal, balanced, and inphase with respect to source voltages. During grid faults, voltage fluctuations at the load terminals are suppressed by maintaining the constant terminal voltage. Load as asynchronous machine i.e, induction motor is considered.

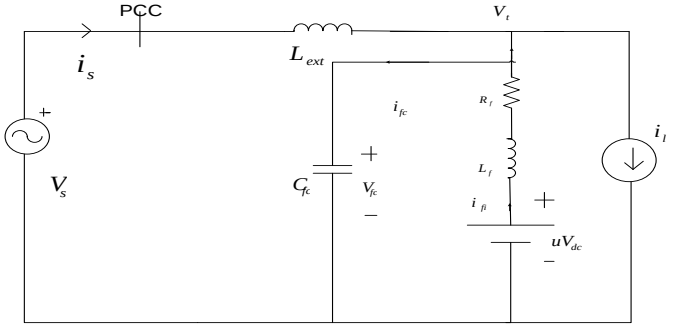

Fig.1. Single phase equivalent circuit of DSTATCOM in a distribution network.

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II. Configuration of DSTATCOM and External inductor selection

Fig.1. Shows the single phase equivalent circuit of DSTATCOM in a distribution network, in which neutral clamped voltage source inverter (VSI) topology is chosen, represented as uV_{dc}.The external series inductance L_{ext} is connected in between the PCC and load terminal. The VSI is connected to load terminals through an LC filter ($L_f - C_{fc}$) [ii-iv]. Voltage maintained across each DC capacitor is considered as V_{dc}. u is a control variable which can be +1 or -1 depending upon switching state.v_s , v_t are source and load voltages respectively.i_{ft},i_{fi} and i_{fc} are currents through DSTATCOM, VSI and C_{fc} respectively.i_s and i_l are source and load currents respectively[ix].

During voltage disturbances external impedance plays a crucial role, the value is decided by the amount of sag to be mitigated and rating of DSTATCOM. Assuming source voltage balanced, source currents at any time and at any phase be given as

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$$\bar{I}_s = \frac{V_s \angle 0 - V_t \angle -\delta}{R_{ext} + jX_{ext}} \quad (1)$$

The RMS source voltage, RMS load voltage, external resistance, external reactance and load angle are represented as $V_s, V_t, R_{ext}, X_{ext}$ and δ respectively. In practical cases, $X_{ext} \gg R_{ext}$. As a design consideration, the reactive source current ($Im[\bar{I}_s]$) supplied by compensator will be maximum when δ is minimum. To this, the VSI losses will be supplied by source only, hence δ will be very small. The reactive source current is given as follows:

$$Im[\bar{I}_s] = \frac{V_t - V_s}{X_{ext}}. \quad (2)$$

To protect the sensitive loads from voltage disturbances, capability of DSTATCOM to mitigate deep sag to be improved. For this 0.9 p.u (per unit) is taken as load voltage during voltage sag, which is sufficient to protect the load. To protect the load from sag of 50%, the reactive current injected by the compensator to be assumed as 20 A. The valve of external reactance is found to be as follows

$$X_{ext} = \frac{0.9-0.5}{20} * 230 = 4.6\,\Omega. \quad (3)$$

NEW CONTROLLER DESIGN

During voltage disturbances, the voltage at the load terminals is regulated by the new controller while retaining the advantages of CCM during normal operation. To get the advantages of CCM operation, the currents drawn from source to be computed and these currents used to compute the magnitude of voltages at the load terminals[x]. In case of voltage disturbance, voltage lies outside the permissible range, and the fixed voltage magnitude is considered as reference voltage. If this voltage magnitude lies within the range, then the same voltage is used as reference voltage. VSI losses and load power extracted from the source through two loop controller using output as load angle. To obtain switching pulses, a discrete model to be derived. Below section represents all steps in a detailed manner.

REFERENCE VOLTAGE MAGNITUDES

In CCM operation, the following advantages to be achieved, even the load voltage is regulated during normal operation. They are as follows

1. Unity power factor to be maintained at PCC.
2. Maintain balanced and sinusoidal source currents.
3. Load average power and VSI losses supplied by the source.

To obtain above objectives, symmetrical component theory is used to get reference source currents. Due to the affect of DSTATCOM, the voltages at the load terminals are balanced and sinusoidal, but switching harmonics are present. These harmonics disturbs the reference source currents. To compute reference source currents (i^*_{sa}, i^*_{sb} and i^*_{sc}), positive sequence components of load voltages ($v^+_{ta1}, v^+_{tb1}, v^+_{tc1}$) are to be extracted. They are as follows:

$$i^*_{sa} = \frac{v^+_{ta1}}{\Delta^+_1}(P_{lavg} + P_{Loss})$$

$$i^*_{sb} = \frac{v^+_{tb1}}{\Delta^+_1}(P_{lavg} + P_{Loss}) \quad (4)$$

$$i^*_{sc} = \frac{v^+_{tc1}}{\Delta^+_1}(P_{lavg} + P_{Loss})$$

P_{lavg}, and $\Delta^+_1 = \sum_{j=a,b,c}(v^+_{tj1})^2$ is the average load power which is calculated by moving average filter (MAF). P_{Loss}, is the total losses in the inverter. It is computed by PI controller and helps in maintaining the average dc-link voltage ($V_{dc1} + V_{dc2}$) at a predefined value ($2V_{dcref}$).

$$P_{Loss} = K_{pdc}e + K_{idc}\int e\ dt \quad (5)$$

Where $e = 2V_{dcref} - (V_{dc1} + V_{dc2}), K_{pdc}$ and K_{idc} are the voltage error of the PI controller, proportional gain and integral gain, respectively. Load terminal Reference voltages can be derived by using reference currents. For fig. 1 apply kirchhoff's voltage law, the equation as follows

$$\bar{V}_s = \bar{I}_s Z_{ext} + \bar{V}_t \quad (6)$$

For unity power factor operation, source voltage and source currents will be inphase. Therefore source voltage is taken as reference. Then it as follows

$$V_s = I_s(R_{ext} + jX_{ext}) + V_t \angle -\delta$$

The load voltage can be computed from source voltage equation as follows:

$$V_t = \sqrt{(V_s - I_s R_{ext})^2 + (I_s X_{ext})^2}. \quad (7)$$

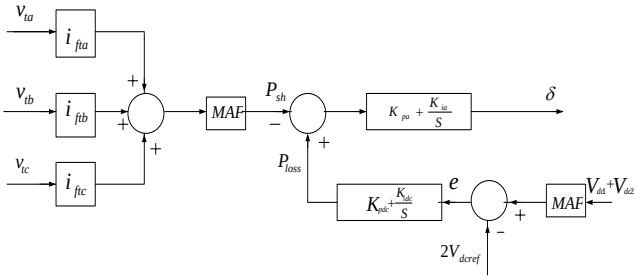

Fig. 2. New controller to calculate δ and P_{Loss} .

Load voltage has a permissible range of variations between 0.9 and 1.1p.u. To achieve the advantages of CCM operation, V_t should be lies within 0.9 and 1.1 p.u and it is taken as reference load voltage (V^*_t). Desired source voltage controls the V_t indirectly. During voltage disturbance i.e, sag and swell, load voltage magnitude is in between 0.9 and 1.1 and 1.1 and 1.8 p.u., respectively, occurs for half cycle to 1 min. Therefore 0.9

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and 1.1p.u is taken as reference load voltage magnitude for sag and swell respectively. The DSTATCOM disturbance withstanding capability is increased by considering load voltage magnitudes to these values. The conclusions[ix] drawn as follows:

$$\text{If } 0.9 \text{ p.u.} \le V_t \le 1.1 \text{ p.u. then } V_t^* = V_t$$
$$\text{Else If } V_t > 1.1\text{p.u then } V_t^* = 1.1 \text{ p.u.} \quad (8)$$
$$\text{else If } V_t < 0.9 \text{ p.u then } V_t^* = 0.9 \text{ p.u.}$$

COMPUTATION OF LOAD ANGLE:

The load angle can be computed from the block diagram of a controller as shown in fig 2. It can be compute by comparing P_{Loss} and P_{sh}.As a result error is generated, then it is passed through PI controller. The load angle (δ) as follows:

$$\delta = K_{pa}(P_{Loss} - P_{sh}) + K_{ia}\int (P_{Loss} - P_{sh})dt \quad (9)$$

Where K_{ia} and K_{pa} are the integral and proportional gains of the inner loop PI controller. MAF is to compute the value of shunt link power. It as follows:

$$P_{sh} = \frac{1}{T}\int_{t1}^{t1+T}(v_{ta}i_{fta} + v_{tb}i_{ftb} + v_{tc}i_{ftc})dt. \quad (10)$$

Power flow from DSTATCOM to load terminal only when the value of P_{sh} is positive, whereas power flow from load terminal to DSTATCOM [vii] when P_{sh} is negative. In steady state P_{sh} is negative because source supply power to compensate the VSI losses[vi]. In steady state capacitor voltage also decreases from its reference value, it represents losses in the VSI. It indicates P_{Loss} will be negative in steady state, due to this P_{Loss} and P_{sh} should be equal and the difference of P_{sh} and P_{Loss} is minimized. Fig.2 represents δ as output of inner PI controller. It indicates that the shunt-link power P_{sh} is equal to losses in the capacitor P_{Loss}.

INSTANTANEOUS REFERENCE VOLTAGE

The three phase reference voltages are considered by selecting a suitable reference load voltage magnitude[14], load angle δ. They are as follows:

$$v_{trefa} = \sqrt{2}V_t^* \sin(\omega t - \delta)$$
$$v_{trefb} = \sqrt{2}V_t^* \sin(\omega t - 2\pi/3 - \delta)$$
$$v_{trefc} = \sqrt{2}V_t^* \sin(\omega t + 2\pi/3 - \delta) \quad (11)$$

Here ω represents frequency of the system.

GENERATION OF SWITCHING PULSES

The discrete model of a single phase has to be derived to generate switching pulses because the each phase of the VSI can be controlled independently. Following equations are obtained from fig.1 for filter inductor and capacitor[vi-vii], they are as follows:

$$\frac{dv_{fc}}{dt} = \frac{1}{C_{fc}}i_{fi} - \frac{1}{C_{fc}}i_{ft}$$
$$\frac{di_{fi}}{dt} = \frac{1}{L_f}v_{fc} - \frac{R_f}{L_f}i_{fi} + \frac{V_{dc}}{L_f}u \quad (12)$$

Above equations represented in matrix form as follows:

$$\dot{x} = Ax + Bz \quad (13)$$

Where

$$A = \begin{bmatrix} 0 & \frac{1}{C_{fc}} \\ \frac{1}{L_f} & \frac{-R_f}{L_f} \end{bmatrix}, \quad B = \begin{bmatrix} 0 & \frac{1}{C_{fc}} \\ \frac{V_{dc}}{L_f} & 0 \end{bmatrix}$$
$$x = \begin{bmatrix} v_{fc} & i_{fi} \end{bmatrix}^t, \quad z = \begin{bmatrix} u & i_{ft} \end{bmatrix}^t$$

The continuous form equation can be represented in discrete form as follows:

$$x(K+1) = Gx(K) + Hz(K) \quad (14)$$

Where G and H are given as

$$G = \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix}, \quad H = \begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix}$$

Therefore voltage across the capacitor will be

$$v_{fc}(K+1) = G_{11}v_{fc}(K) + G_{12}i_{fi}(k) + H_{11}u(K) + H_{12}i_{ft}(K) \quad (15)$$

The reference voltage v_{tref} is maintained at the load terminal. J is chosen as a cost function

$$J = \left[v_{tref}(K+1) - v_{fc}(K+1)\right]^2. \quad (16)$$

The condition for cost function minimization is

$$v_{fc}(K+1) = v_{tref}(K+1). \quad (17)$$

Therefore, the reference discrete voltage control law from eqns is

$$u^*(K) = \frac{v_{tref}(K+1) - G_{11}v_{fc}(K) - G_{12}i_{fi}(K) - H_{12}i_{ft}(K)}{H_{11}} \quad (18)$$

To generate switching pulses of VSI, $u^*(K)$ is regulated around a hysteresis band h using hysteresis control [vii-ix].

III. Results and Discussions

The proposed new controller and multifunctional DSTATCOM make three phase source currents balanced, sinusoidal, and in phase with respective source voltages at the PCC, within the permissible range of voltage. During voltage disturbances fast voltage regulation is provided to protect the sensitive loads at the load terminals. In addition, reactive current and load harmonic components are supplied by the compensator all the time. A three phase stiff source of 230 V rms per phase (1.0 p.u.) is considered. Filter parameters are L_f = 20mH, C_f =10μF, V_{dc}= 800 V,
and C_{dc} =3000μF.

Initially, a three phase unbalanced nonlinear load is connected. For achieving multifunctional DSTATCOM operation three phase fault is created at source side. When three phase fault exist on line at t=0.2 to 0.25 sec, following power quality issues arise as follows:

SAG RESULTS

From Fig (3) it is observed that, time t=0.2 to 0.25 sec, sag has appeared on induction motor. During sag period, source current will increase as shown in fig. 3(a). New controller multifunctional DSTATCOM maintains the load current across

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the induction motor without any variation from previous condition, at the same time constant voltage is maintained at the induction motor. Consequently the source current and the source voltage slowly come in phase with each other. Fig (5) (a) shows the stator current of an induction motor, starting inrush currents settles after sag period. Speed and torque of an induction motor observed in Fig (5)(b)and (5)(c). Fig. 4. represents voltage across DC capacitor.

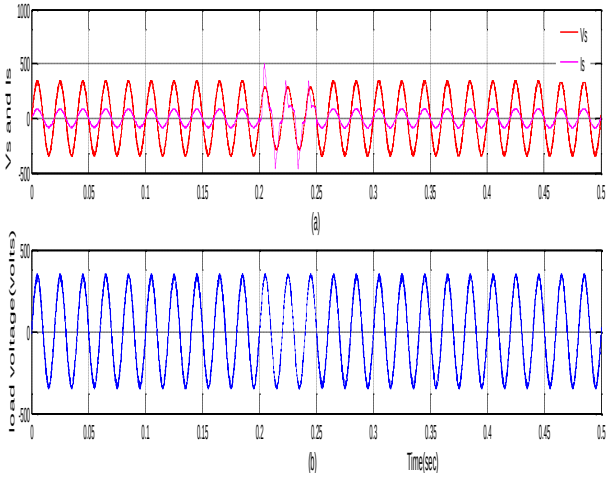

Fig 3. phase-a waveforms before, during and after sag. (a) Source voltage and source current. (b) Load voltage.

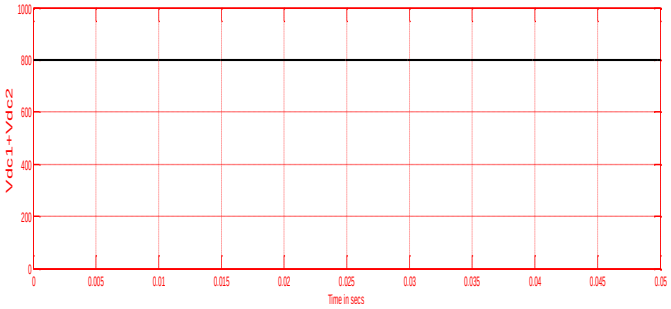

Fig 4. DC bus voltage.

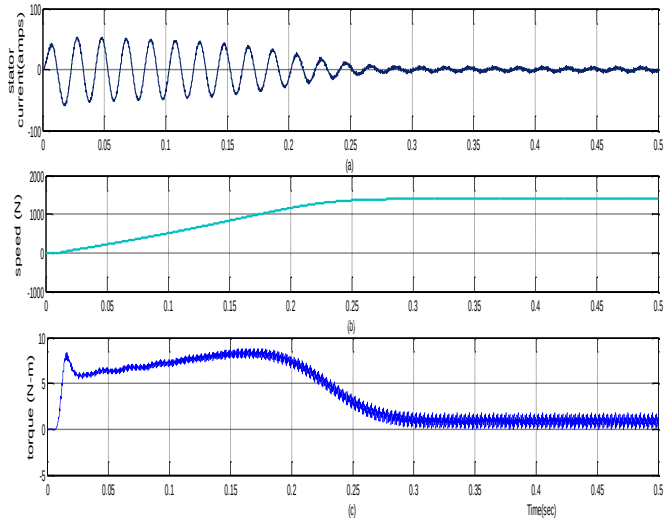

Fig.5. (a) Stator current, (b) speed, (c) torque of an induction motor.

IV. Conclusion

In this paper, a new controller based multifunctional DSTATCOM has been proposed to protect the load from voltage disturbance under stiff source. By operating the DSTATCOM in CCM and VCM, mainly power quality issues of sag compensated and protect the load. The proposed controller and multifunctional DSATCOM are able to mitigate voltage and current-related power quality issues, and confirmatory results are presented.

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