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A New Fangled Approximate Compressor Design for Multiplication

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Abstract: In this paper, a novel implementation of 4*4 Multiplier using 4-2 Approximate Compressors is presented; which produces quick results, especially for use in Digital Signal Processors and in Microprocessors. We propose 3 approximate 4-2compressor designs which provide better area, power consumption, critical path delay and less number of transistor counts when compared to the exact 4-2compressor designs. Here we used the proposed designs in the multiplication applications, of DADDA tree& WALLACE tree. Dadda tree multiplier is faster than Wallace tree multiplier. Compressors decrease the complexity of multiplier, power consumption and increase the speed by reducing delay with the diminish cost of error rate. Hence, instead of using conventional methods such as approximate compressors used for multiplication. All the circuits are designed and simulated using DSCH and MICROWIND tool.

KEY WORDS-Exact Compressor, Approximate compressor, Dadda multiplier, Wallace multiplier

I INTRODUCTION

The multipliers concert helps in determining the processor's speediness of running and performance of the DSP algorithms. In most of the VLSI systems, multiplier factor directly lies within the critical path. For these reasons, the designers continually focus on developing multipliers of high speed, low power delay power efficiency circuits. In digital signal processing & image multiplication, Multipliers plays an important role. But nonetheless multipliers inhibit more area & incur longer delays than adders. Hence it is imperative to extend special techniques to speed up the multiplication operation. By this area problem conquer.

Multiplication involves mainly 3 steps

1) Partial product generation
2) Partial product reduction
3) Final addition

Among these three phases, the second phase - partial product reduction phase consumes most of the power and is responsible for overall critical path delay. Therefore in order to organize this stage, Compressors can be used for partial product accumulation. To design high speed and low power multiplier, compressors have been widely used. To speed up the partial product reduction, by reducing number of stages power dissipation drastically reduces.

A compressor is a single bit adder circuit that has more than three inputs as in full adder and sum& carry as outputs. Compressor compresses four partial products into two. (Sum&carry). To acquire fewer interconnections employ of compressors is very important. If the addends are four or more, then one layer of compressors is necessary, and there are various possible designs for the circuit, the most common are Dadda and Wallace trees. There are different types of compressors are available such as 3-2 compressor, 4-2 compressor. This kind of circuit is most notably used in multipliers to reduce partial products. Compressors reduce the complexity of multiplier, power consumption and increase the speed by reducing delay with the diminish cost of error rate. Hence, instead of using conventional methods such as approximate compressors used for multiplication.

This paper is organized as follows: In section 2, composition of 4-2 Compressor and its design is described. In section 3, proposed approximate compressors designs are discussed. In section 4, based on the proposed designs DADDA & WALLACE tree multipliers are designed. In section 5 Experimental results and evaluation of our scheme DADDA multiplier are presented & compared. Finally, we conclude this work in Section 6.

II EXISTING COMPRESSOR CIRCUIT

A. Exact 4-2 compressor

The main goal of either multi-operand carry save addition or parallel multiplication is to reduce n numbers to numbers to two numbers; consequently n-2 compressors (n-2 counters) have been extensively utilized in computer arithmetic.

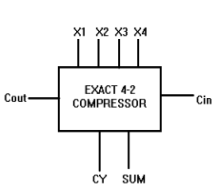

Fig1. EXACT compressor

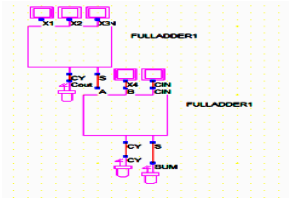

Fig2. Implementation of 4-2 compressor

A widely used structure for compression is the 4-2 compressor; that can be shown in a 4-2 compressor (Fig2.) can be implemented with a carry bit between adjacent slices (ξ=1). The carry bit from the position to the right is denoted as Cin while the carry bit into the higher position is denoted as Cout. The two output bits in positions i and i + 1 are also referred to as the sum and carry respectively. The following equations give the outputs of the 4-2 Compressor.

$$Sum = X1 \oplus X2 \oplus X3 \oplus X4 \oplus Cin \quad (1)$$

$$Cout = (X1 \oplus X2)\,X3 + (\overline{X1 \oplus X2})\,X1 \quad (2)$$

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$$Carry = (X1 \oplus X2 \oplus X3 \oplus X4)\, Cin + \overline{(X1 \oplus X2 \oplus X3 \oplus X4)}X4 \qquad (3)$$

Actually the exact compressor (fig b) can be developed by using two full adders. In this totally 4 inputs (Cin is internal input) & three outputs (sum, carry, Cout) are available.

B. Optimized 4-2 compressor

The optimized design of 4-2 compressor is insist of 4 XNOR gates & 2 MUXes. In this 2-1 multiplexer is used to develop compressor.

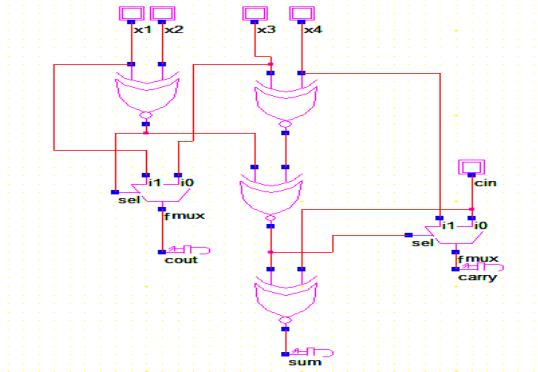

Fig3. Optimized 4-2 compressor

This posses less delay when compare to other circuits. The critical path delay for this circuit is 3 Δ. Here Δ is the unitary delay through any gate. Here totally 32 combinations are available. By the availability of 32 combinations the number of inputs, outputs, transistor count & power consumption is more.

III PROPOSED APPROXIMATE COMPRESSOR

Three approximate compressors designs intended in this segment. Two level approximations utilize little bits to acquire the simple circuit. However the exact compressor attains from optimized produces at least 17 incorrect results out of 32 possible outputs. i.e., error rate is 53% (error rate
is the ratio of no. of erroneous outputs to the total no. of outputs). To diminish error rate assort designs are developed, which offers astonishing performance improvement while compared to an exact compressor with respect to delay,area,power consumption.

A. Design 1 Approximate compressor

To reduce the error rate & enhance the performance Design 1 is proposed. To obtain a simplified circuit based on the k-map (octet, quad, pair groups) sum & carry modified. By this the obtained sum & carry are as follows. Here 2XNOR, 3NOR&1 OR gate is used.

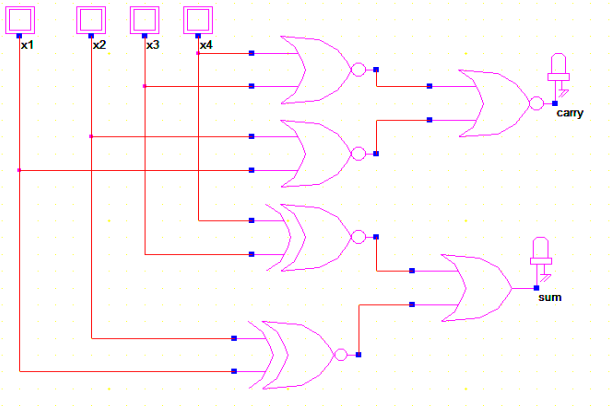

Fig4. Design 1 approximate compressor

The gate level implementation of approximate compressor is shown in fig4. The critical path delay for design 1 is 2 Δ , so it is 1 Δ less than preceding design. The block diagram & truth table of design 2 is shown below.

This design produces 4 incorrect outputs out of 16 outputs, the error rate also reduced to 25%. This is very positive feature.

B. Design 2 Approximate compressor

In design 2 carry similar to the design 1, but to reduce error rate% sum only modified. Design2. uses 3 XOR, 3 NOR gates. This gives 2 incorrect outputs out of 16 inputs. In this design 2 the error rate is 12.5% only.

$$Sum = (X1 \oplus X2) \oplus (X3 \oplus X4) \qquad (6)$$

$$Carry = \overline{(\overline{X1X2} + \overline{X3X4})} \qquad (7)$$

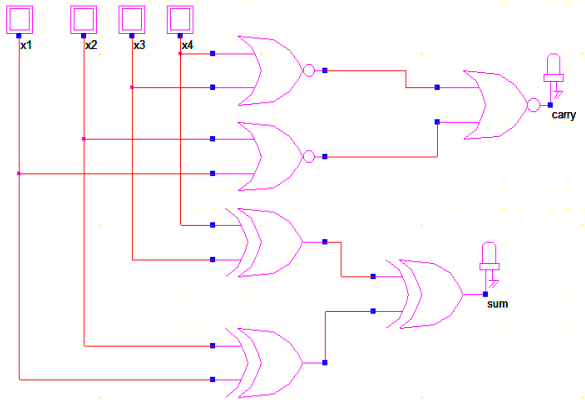

Fig5. Design 2 approximate compressor

C. Design 3Approximate compressor

Here sum is similar to the Design 2 but carry modified. In design 3 the error rate is 6.25% only. By using this circuit in multiplication better results are obtained.

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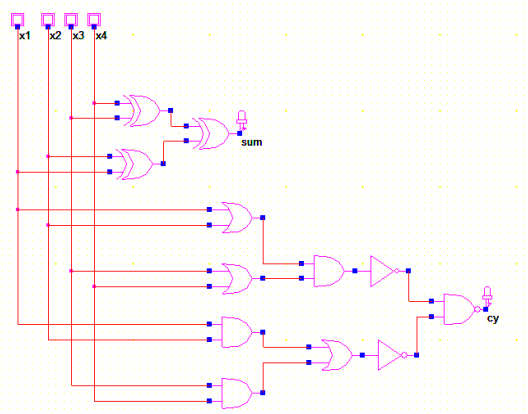
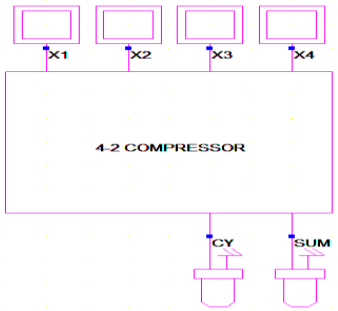
$$Sum = (X1 \oplus X2) \oplus (X3 \oplus X4) \quad (8)$$

$$Carry = \overline{((X1 + X2)\ (X3 + X4))}\ \overline{(X1X2 + X3X4)} \quad (9)$$



a)



b)

Fig6.a) Design3 approximate compressor
b) Approximate 4-2 compressor

The approximate compressor des 2 truth table is shown below. This table shows the decimal value of the addition of inputs & outputs difference. For example when all inputs are 1, the decimal value count of the inputs is 4. However approximate compressor produces a 1 for carry& 1 for sum. The decimal value for this is 3; in this case difference is-1.But it takes more area and power consumption. Among all three designs Design 2 is better performance provider.

Table 1:

Truth table of design 3 approximate 4-2 compressor

X4	*X3*	*X2*	*X1*	*carry*	*sum*	*difference*
0	0	0	0	0	0	0
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	0	-2
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	1	0
1	0	0	0	0	1	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	0	-2
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	-1

IV MULTIPLICATION

The tree (parallel) multipliers are generally highly performance efficient. In these tree multipliers, first phase of partial product generation is implemented by multiplying each multiplicand bit with the multiplier bit by AND operation. The Tree multipliers like Wallace and Dadda differ mainly in the Partial product reduction phase based on the type of reduction algorithm used. The last addition phase performs addition of the reduced bits using Carry Propagate Adder (CPA) to produce the final result. Wallace & Dadda are tree multipliers, used to improve the speed.

Multipliers built from Approximate 4-2 compressors

By using Compressors in partial product reduction phase in multipliers will help to produce lesser number of interconnections and adder cells.

A. Wallace Tree Multiplier using approximate 4-2 Compressors

The design of 8x8 Wallace Multiplier using 4-2 compressors is shown in Figure7. By using compressors the number of reduction stages gets reduced to 3, instead of 5 stages when only half and full adders are used. The delay and thus PDP also gets reduced. The Multiplier uses 17 no. of 4-2 Compressors, 18 full adders and 9 half adders. This Wallace tree has lesser delay compared to the one which does not use 4-2 compressors. But it uses full adders whenever possible to maintain predetermined stage.

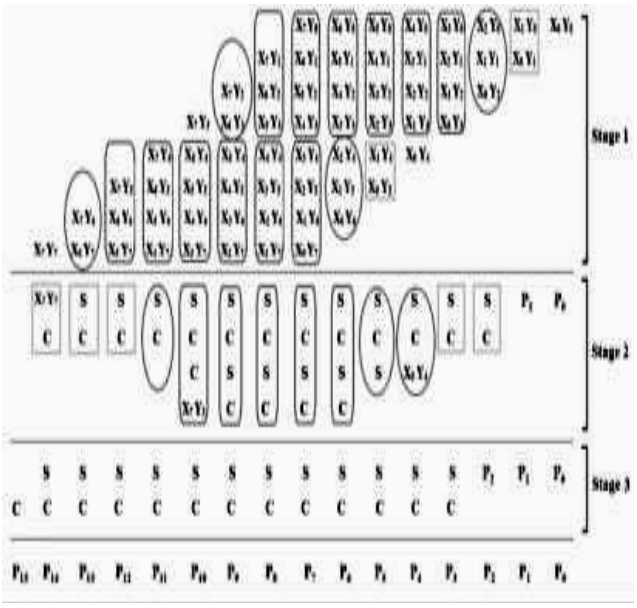


Fig7; 8*8 WALLACE TREE MULTIPLIER

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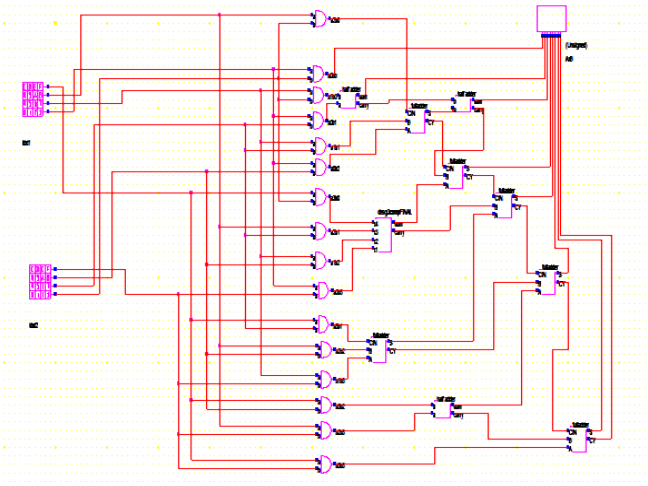
Architecture of 4*4 WALLACE tree multiplier using Design2.



B. DADDA Tree Multiplier

Luigi Dadda, the computer scientist has invented the DADDA hardware multiplier during 1965. DADDA multiplier is extracted form of parallel multiplier. It is slightly faster and requires fewer gates. This scheme essentially minimizes the number of adder stages required to perform the summation of partial products.

Dadda multiplication performed as follows

- Each bit of one argument multiply with each and every bit of other argument, action performs until all arguments are multiplied.
- If availability of products are 4then it use compressor, if it is two then it uses half adder, if it is three uses full adder.
- The main aim of this is to reduce all partial products into two numbers for simplification.
- Finally addition performs by conventional adder.

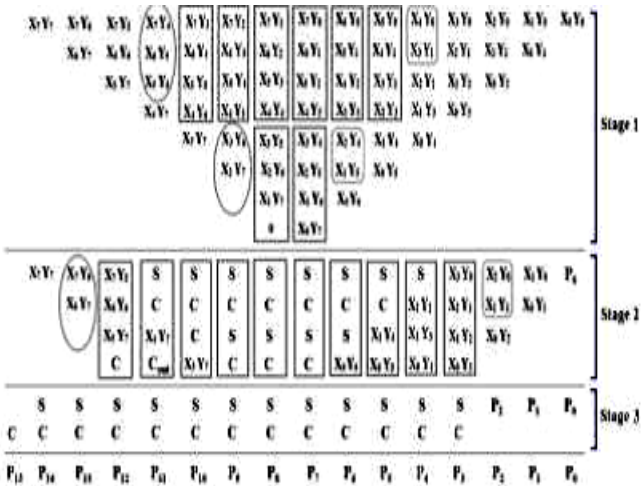
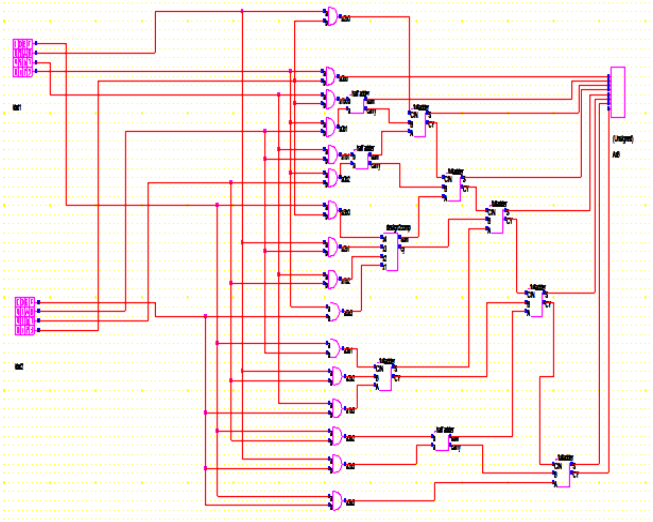


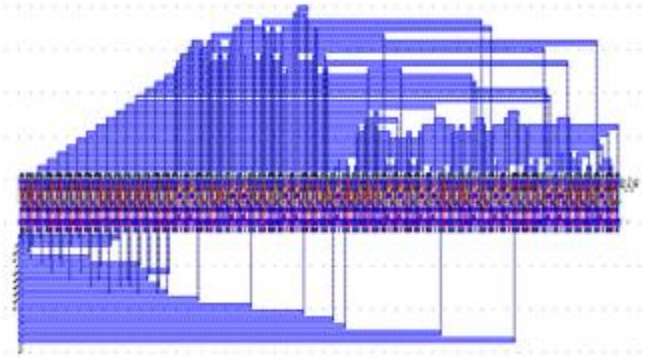
Fig8; 8*8Daddatree Multiplier

Architecture of 4*4 DADDA tree multiplier using Design2.

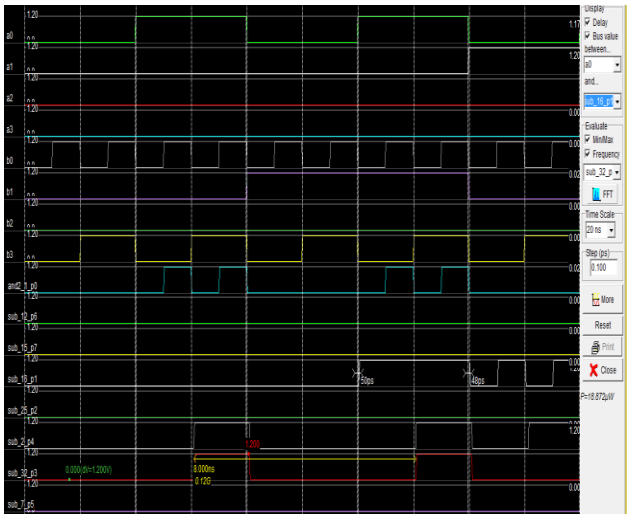


V THE SIMULATION RESULTS

LAYOUT OF 4*4 DADDA multiplier



The simulation results of 4*4 DADDA multiplier



The comparision results of exact & approximate compressors are shown below in table2.

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Table2.

Compressor type	Power(μw)	Area(μm^2)	Critical path(ns)
Des1	5.521	220	0.604
Des2	2.399	160	0.184
Des3	9.224	216	0.076
Exact compressor	6.531	434	0.280
Optimized compressor	7.391	403	0.910

Among all of these compressor designs the proposed designs provides better results when compare to the exact compressors.So, DADDA&WALLACE multipliers can be designed with the help of proposed designs & simulated results are given below table3.

Table3.

Compressor type	Multiplier type	Area(μm^2)	Power(μw)	Critical path(ns)
Des1	Dadda tree multiplier	2108	23.483	0.340
	Wallace tree multiplier	3192	25.163	0.532
Des2	Dadda multiplier	1938	18.872	0.304
	Wallace tree multiplier	3013	29.821	0.449
Des3	Dadda multiplier	2527	26.442	0.489
	Wallace tree multiplier	2680	32.184	0.499

VI. CONCLUSION

Thus we conclude that faster multipliers can be designed with the use of 4-2approximate compressors for partial production reduction stage of Dadda multiplier& Wallace multiplier. When the Simulation results were performed using microwind at 90nm CMOS technology, the 4*4 Dadda multiplier shows optimal speed performance against Wallace Tree Multiplier implemented with 4-2 Approximate Compressors provides less power consumption, area & less critical path. This proposed reduction format can also be applied to higher order NxN multipliers for high speed results & less power consumption.

REFERENCES

i) Z. Wang, G. A. Jullien, and W. C. Miller, ―A new design technique for column compression multipliers,‖ IEEE Trans. Computers, vol.44, pp.962-970. Aug 1995.

ii) Chip-Hong Chang, *Senior Member, IEEE*, Jiangmin Gu, Ultra Low-Voltage Low-Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 51, NO. 10, OCTOBER 2004.

iii) S.F. Hsiao, M.R. Jiang, J.S. Yeh, ―Design of high low power 3-2 counter and 4-2 compressor for fast multipliers‖, Electronic Letters, Vol. 34,No. 4, pp. 341-343, 1998.

iv)J. Ma, K. Man, T. Krilavicius, S. Guan, and T. Jeong, "Implementation of High Performance Multipliers Based on Approximate Compressor Design" in international Conference on Electrical and Control Technologies (ECT), 2011.

v) Baran, Dursun, Mustafa Aktan, and Vojin G. Oklobdzija. "Energy efficient implementation of parallel CMOS multipliers with improved compressors."*Proc. of the 16th ACM/IEEE international symposium on Low power electronics and design*. ACM, 2010.

vi)c.Chang, J. Gu, M. Zhang, "Ultra Low-Voltage Low- Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits," *IEEE Transactions on Circuits & Systems*, Vol. 51, No. 10, pp. 1985-1997, Oct. 2004.

vii) A. Momeni, J. Han, P. Montuschi and F. Lombardi,''Design and Analysis of Approximate Compressors for Multiplication'', IEEE Trans. Computers, vol. 64, no. 4, pp.984-994, April 2015.

viii)D. Radhakrishnan and A.P. Preethy, "Low-power CMOS pass logic 4-2 compressor for high-speed multiplication," in *Proc. 43rd IEEE Midwest Symp. Circuits Syst.*, vol. 3, 2000, pp. 1296–1298.

ix)L.S. WALLACE "A suggestion for fastmultipliers,"IEEE Trans .comput.,vol. EC-13, pp. 14-17,Feb. 1964.