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Migration from Hardware to Software Radio

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Abstract: Radio is a hardware device which operates in the radio frequency part of electromagnetic spectrum and facilitates communication. There are a variety of standards in commercial use to establish communication through their specific application. Traditional radio devices limit cross-functionality and demonstrate minimal flexibility in supporting multiple waveform standards. Software Defined Radio (SDR) technology provides an efficient solution by allowing a multiband, multistandard, multiservice and multichannel system which can be reconfigured for interstandard handover.

I. INTRODUCTION

The SDR Forum, working in collaboration with the Institute of Electrical and Electronic Engineers (IEEE) P1900.1 group, has worked to establish a definition of SDR as:"Radio in which some or all of the physical layer functions are software defined". SDR defines a collection of hardware and software technologies where some or all of the radio's operating functions (also referred to as physical layer processing) are implemented through modifiable software or firmware operating on programmable processing technologies. These devices include field programmable gate arrays (FPGA), digital signal processors (DSP), general purpose processors (GPP), programmable System on Chip (SoC) or other application specific programmable processors. The use of these technologies allows new wireless features and capabilities to be added to existing radio systems without requiring new hardware.[1][2]

II. WORKING OF HARDWARE RADIO

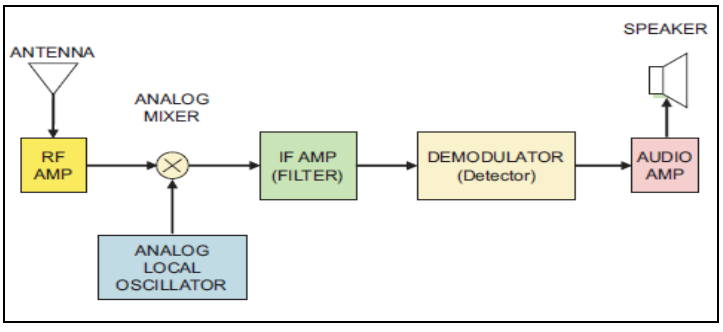

Figure 1-Analog Radio Receiver Block Diagram

The conventional heterodyne radio receiver is shown in Figure 1. First the RF signal from the antenna is amplified, typically with a tuned RF stage that amplifies a region of the frequency band of interest. This amplified RF signal is then fed into a mixer stage. The other input to the mixer comes from the local oscillator whose frequency is determined by the tuning control of the radio. The mixer translates the desired input signal to the IF (Intermediate Frequency). The IF stage is a bandpass amplifier that only lets one signal or radio station through. The demodulator recovers the original modulating signal from the IF output using one of several different schemes. The demodulated output is fed to an audio power amplifier which drives a speaker. The mixer performs an analog multiplication of the two inputs and generates a difference frequency signal. This is called "downconversion" or "translation" because a signal at a high frequency is shifted down to a lower frequency by the mixer.

III WORKING OF SDR

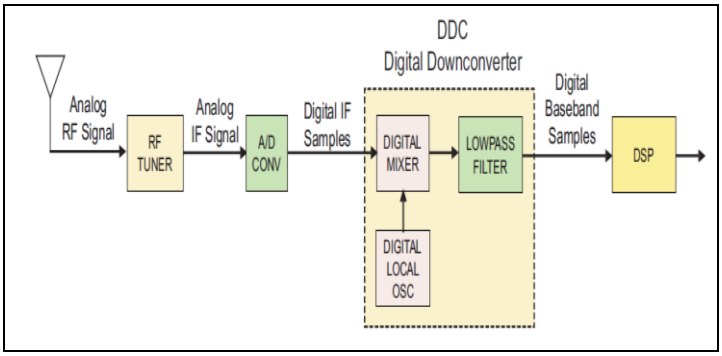

Figure 2-SDR Receiver block diagram

Figure 2 shows a block diagram of a software defined radio receiver. The RF tuner converts analog RF signals to analog IF frequencies, the same as the first three stages of the analog receiver. The A/D converter that follows digitizes the IF signal thereby converting it into digital samples. These samples are fed to the next stage which is the digital downconverter (DDC) shown within the dotted lines. The digital downconverter is typically a single monolithic chip or FPGA IP, and it is a key part of the SDR system. A conventional DDC has three major sections: digital mixer, digital local oscillator and FIR lowpass filter. The digital mixer and local oscillator translate the digital IF samples down to baseband. The FIR lowpass filter limits the signal bandwidth and acts as a decimating lowpass filter. The digital downconverter includes a lot of hardware multipliers, adders and shift register memories to accomplish the task. The digital baseband samples are then fed to a block labeled DSP which performs tasks such as demodulation, decoding and other processing tasks. Traditionally, these needs have been handled with dedicated application-specific ICs (ASICs), and programmable DSPs. At the output of the mixer, the high frequency wideband signals from the A/D input have been

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translated down to DC as complex I and Q components with a frequency shift equal to the local oscillator frequency. This is similar to the analog receiver mixer except there, the mixing was done down to an IF frequency. Here, the complex representation of the signal allows to go right down to DC. By tuning the local oscillator over its range, any portion of the RF input signal can be mixed down to DC. In effect, the wideband RF signal spectrum can be "slid" around 0 Hz, left and right, simply by tuning the local oscillator. The DDC performs two signal processing operations: (a) Frequency translation with the tuning controlled by the local oscillator, (b) Lowpass filtering with the bandwidth controlled by the decimation setting.

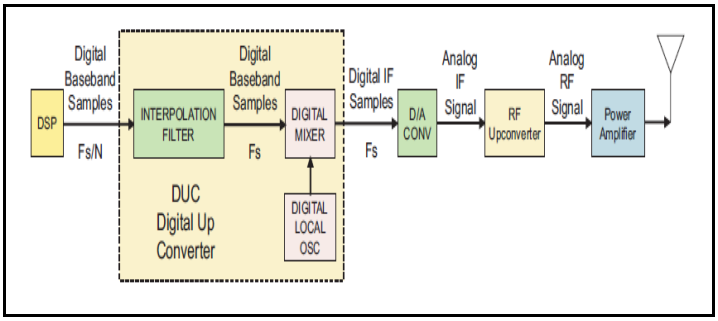

Figure 3-SDR Transmitter Block Diagram

The input to the transmit side of an SDR system is a digital baseband signal, typically generated by a DSP stage as shown in Figure 3 above. The digital hardware block in the dotted lines is a DUC (digital upconverter) that translates the baseband signal to the IF frequency. The D/A converter that follows converts the digital IF samples into the analog IF signal. Next, the RF upconverter converts the analog IF signal to RF frequencies. Finally, the power amplifier boosts signal energy to the antenna. Inside the DUC shown in Figure 14, the digital mixer and local oscillator at the right translate baseband samples up to the IF frequency. The IF translation frequency is determined by the local oscillator.

Key DDC and DUC Benefits - Think of the DDC as a hardware preprocessor for programmable DSP or GPP processor. It preselects only the signals you are interested in and removes all others. This provides an optimum bandwidth and minimum sampling rate into the processor. The same applies to the DUC. The processor only needs to generate and deliver the baseband signals sampled at the baseband sample rate. The DUC then boosts the sampling rate in the interpolation filter, performs digital frequency translation, and delivers samples to the D/A at a very high sample rate. The number of processors required in a system is directly proportional to the sampling frequency of input and output data. As a result, by reducing the sampling frequency, you can dramatically reduce the cost and complexity of the programmable DSPs or GPPs in the system. DDCs and DUCs enabled reduction of bandwidth and sampling rate helps save time in data transfers to another subsystem. This helps minimize recording time and disk space, and reduces traffic and bandwidth across communication channels.[3]

A comparison between hardware and software defined radio is given below in Table 1:-

Criteria	Hardware Radio	SDR
Complexity	Less	More
Flexibility	Less	More
Portability	Less	More
Power Consumption	Less	More

Table 1-Comparison of Hardware radio and SDR

IV. SDR MODULES AND HARDWARE

The main hardware alternatives that can be used to implement a SDR are ASICs (Application-Specific Integrated Circuits), FPGAs (Field-Programmable Gate Arrays), DSPs (Digital Signal Processors) and GPPs (General-Purpose Processors).

General Purpose Processors-A general purpose processors (GPP) is a typical microprocessor, like the ones powering personal computers. As the name implies, these devices are optimized to handle the widest possible range of applications. GPPs must excel at fixed and floating-point operations, logical operations, and branching. This makes them suitable for implementing much of the SDR functionality, starting with the physical layer DSP and ending with the protocol and network stacks. GPPs provide the easiest development environment and highest developer productivity. The largest pool of qualified developers is familiar with GPPs. The development tools and expertise apply to GPPs from different vendors and product lines. A wide range of operating systems is also available. These advantages make GPPs the easiest platform for SDR development.

Digital Signal Processors-A digital signal processors (DSP) is a microprocessor that is optimized for number crunching. Manufacturers of DSP devices can optimize them for a much narrower set of target applications than GPPs. Power consumption can be reduced by eliminating transistors that a GPP has to devote to sophisticated cache and peripheral subsystems. The main advantage of DSPs over GPPs is in power consumption per operation. DSPs come in both fixed- and floating-point varieties, with fixed-point versions offering even lower power consumption. DSPs are not well suited for control intensive code such as the protocol and network stack. A typical SDR would pair a DSP with a GPP to implement the network stack. The development environment for a DSP is somewhat more complex than for a GPP. Operating system support is also significantly more limited, with many DSP projects not using any OS at all and interacting with the hardware directly. DSP developers are significantly more difficult to find than GPP developers. Optimal use of a DSP requires the developer to be very familiar with the internal architecture, and the expertise in one family does not translate to another family. DSPs are used extensively in software-defined cellular base stations and in radios that require low power and have modest data rate requirements.

Field Programmable Gate Arrays-A field programmable gate array (FPGA) is a microchip that is designed to be configured by the user after manufacture. An unconfigured FPGA has absolutely no functionality. FPGAs contain programmable logic components called ‘‘logic blocks’’ and reconfigurable interconnect to ‘‘wire’’ the blocks together. Logic blocks can be configured to perform complex combinational functions or simple logic such as AND, NOT, XOR, etc. Each logic block is usually paired with one or more registers to store the result. Most FPGAs also include large ‘‘macro blocks’’ for frequently used functions such as memory blocks, multipliers, interfaces to external devices, and even complete microprocessors. FPGA vendors differentiate themselves by providing the right mix of logic and macro blocks. FPGAs consume significantly more power than an equivalent single function design. Designs implemented on an FPGA also execute a lot slower than an equivalent single-function design.

Specialized Processing Units(SPU)-A number of devices suitable for DSP do not fall neatly into any of the categories above. Specialized processing units (SPUs) typically combine multiple cores with different characteristics to allow efficient mapping of SDR algorithms.[4]
Comparison between various parameters of GPP, DSP and FPGA is given in Table 2:-

Parameter	GPP	DSP	FPGA
Power Consumption	Moderate	High	Low
Development environment	Easiest	Complex	Complex
OS Support	Available	Limited	Available
Speed	Faster	Faster	Fast
Configurability	Easy	Easy	Complex

Table 2-Comparison between GPP, DSP and FPGA

Table 2 shows the comparison between DSP, GPP and FPGA. DSPs are microprocessors with architecture, instructions and features suited specifically for signal processing applications. DSP and GPPs are essentially serial in operation. The main strengths of DSPs and GPPs are their flexibility and easy configurability. Field Programming Gate Arrays (FPGA) contains DSP blocks that can be re-configured to work as parallel multiplier/adder or MAC. FPGA are extremely flexible and fast as they provide high computing power due to quasi-parallel processing nature.

V ROADMAP FOR SDR DEPLOYMENT

SDR Technology is a concept or enabler rather than a system implementation. There will be system implementations based on SDR Technology (for example cognitive radios) as well as equipment enhanced with SDR capabilities. To be able to distinguish the different implementation types, the SDR Forum introduced a classification scheme for radios.[5] The scheme identifies the levels of configurability and reconfigurability as outlined in Table 3:-

Level	Type of Radio	Reconfigurability
0	HW (Hardware Radio)	Reconfiguration through exchange of hardware components only
I	SCR (Software Controlled Radio)	Reconfigurations through control functions in software, limited to pre-defined set of configurations
II	SDR (Software Defined Radio)	Software control and reconfigurability of a variety of modulation techniques (waveforms)
III	ISR (Ideal Software Radio)	Analogue conversion takes place at antenna, speaker and microphone, everything else is digitised and software configurable
IV	Ultimate Software Radio	Understands all traffic and control information and supports (most) applications and radio air interfaces. Although this classification scheme can limit the problems for certification (or type approval) of class 0 and class I equipment, classes II, III and IV provide too much flexibility to be easily and quickly (i.e. in run-time) certifiable (with every change of config).

Table 3: SDR Forum Classification of Radios

VI RESULTS

The migration of radio from hardware to software based architecture has been gradual and it is still in progress round the globe. Use of software defined radio has enabled to reduce the clutter of radio equipments. The characteristics of a SDR is superior in technical capability and performance as indicative in the comparison drawn in the paper. The benefits of SDR are compelling. For Radio Equipment Manufacturers and System Integrators, SDR enables a family of radio “products” to be implemented using a common platform architecture, allowing new products to be more quickly introduced into the market. It allows software to be reused across radio "products", reducing development costs dramatically. Over-the-air or other remote reprogramming allows "bug fixes" to occur while a radio is in service, thus reducing the time and costs associated with operation and maintenance. For Radio Service Providers, SDR enables new features and capabilities to be added to existing infrastructure without requiring major new capital expenditures, allowing service providers to quasi-future proof their networks. The use of a common radio platform for multiple markets, significantly reducing logistical support and operating expenditures. For End Users SDR technology aims to reduce costs in providing end-users with access to ubiquitous wireless communications – enabling them to communicate with whomever they need, whenever they need to and in whatever manner is appropriate. However, even medium performance SDR tends to require more power for a given function than equipment designed specifically for purpose with optimum

analogue/ digital architectural partitioning. Ultra Low Power equipments not requiring large software communication architecture, radio frequency application frequency ranges or modulation types are currently still better implemented in conventional architectures.

In the hardware architecture, the main issues in developing of SDR platform architecture are ADC/DAC sampling rate and computation capacity of processor. To reduce computation complicity, one places the ADC/DAC component in IF section, so the hardware architecture is more realistic.

Current SDR implementations mostly rely on reconfigurable hardware to support a particular standard or waveform while the algorithms and the various setups for other waveforms are stored in memory. Although application-specific integrated circuits lead to the most efficient implementation of a single-standard radio, the same cannot be said when addressing a multi-mode multi-standard device. For a device with such versatility, the ASIC is very complex in terms of implementation and inefficient in terms of cost and power consumption. For this reason, SDR designers have turned to FPGAs to provide a flexible and reconfigurable hardware that can support complex and computationally intensive algorithms used in a multitude of voice, data, and multimedia applications. One or more FPGAs are typically used in conjunction with one or more DSPs, and one or more GPPs and/ or microcontrollers to simultaneously support multiple applications. The comparison of various hardware module also indicate a mix of components to achieve the best characteristic feature in implementing a SDR. Within a SDR, the radio contains several processing elements (GPPs, DSPs, and FPGAs) that can be programmed by the waveform to deliver the required functionality. However, if each waveform must be tailored to the unique capabilities of each individual platform, (e.g., the type of GPP, DSP, and FPGA), significant portions of the waveform may have to be rewritten if they need to be ported to different hardware platforms. As a result, the move toward SDRs has prompted the development of open standards, to make it easier to develop waveforms that can run on multiple platforms with minimal change.

VI CONCLUSION

In this paper a comparative study of the hardware and software radio has been carried out. Also, the choice of hardware instrumental in implementation of SDR has been deliberated upon. The SDR is cleary the next generation radio as it captures all desirable features in a portable size to make available at the disposal of various segment of users. A combination of GPPs, DSPs and FPGAs presently constitutes a successful SDR which supports open standards for interoperability.

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