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A Digital Error Correction Technique for the Resettable Delta-Sigma Modulator Used in a Multiple-Sampling Based High-Resolution ADC

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Abstract:This paper presents a technique for digital error correction of the nonlinearity due to capacitor mismatch and finite gain error of operational amplifier in the first-order resettable delta-sigma modulator (RDSM) used in a multiple-sampling based high-resolution ADC. The effectiveness of the digital error correction is confirmed by using circuit simulation data with 65 nm technology parameters. The simulation results show that the digital error correction improves the integral nonlinearity (INL) from +4.52/-4.58 LSB to +0.30/-0.45 LSB at 12bits.

***Key Words*— Resettable delta-sigma modulator, digital error correction**

I. INTRODUCTION

Analog-to-digital converters (ADCs) using multiple sampling of the input signal are useful for column implementation of the ADC in CMOS image sensors [i, ii, iii]. It provides an advanced function in CMOS image sensors, particularly for noise reduction and extended dynamic range. The multiple-sampling based ADC also known as an extended counting ADC [iv, v, vi] uses a resettable delta-sigma modulator (RDSM), a counter for the comparator (one-bit sub-ADC) output and another ADC used for the analog output of the RDSM for extended conversion. The high-gain amplification of the input by the multiple-sampled integration and folding-integration characteristics of the RDSM provides low-noise and wide dynamic range characteristics of the ADC. For the column implementation of the ADC in CMOS imagers, small-size sampling capacitors and an operational amplifier (op-amp) with simplified circuit configuration are desired in the RDSM for embedding it in a small column pitch, and reducing the area and power consumption of the ADC. However, capacitor mismatch due to the small-size sampling capacitors and the poor DC open-loop gain of the op-amp causes poor linearity of the ADC. The errors which causes nonlinearity of the ADC must be corrected by using error calibration techniques if such poor analog components are used for the low-power area-efficient design of the ADC [vii].

In this paper, a digital error correction technique for the multiple-sampling based high-resolution ADC is proposed. The proposed technique calibrates the analog error of the RDSM in digital domain. To do this, a model of analog errors due to capacitor mismatch of the sampling capacitors and open-loop DC gain of op-amp is built and the errors are corrected in digital domain by finding the best error coefficients to minimize the integral nonlinearity. The effectiveness of the error collection technique is confirmed by doing the digital error correction using an error model of the ADC implemented by MATLAB and using circuit simulation data with 65 nm technology parameters.

II. ADC ARCHITECTURE AND ERROR MODELING

2.1 Entire ADC architecture and operation

The block diagram of the ADC architecture using multiple sampling of input signal is shown in Fig. 1[i, ii]. It consists of a first-order resettable delta-sigma modulator (RDSM), a digital counter as a decimation filter for the coarse ADC output, and an extended ADC for the analog output of the RDSM to generate fine ADC code. This ADC architecture is effective for an input signal which takes a different DC level every one cycle of the A/D conversion. A typical example of this type of signal is the pixel output of CMOS image sensors and the multiple-sampling based ADC is effectively used for low-noise and wide-dynamic-range signal readout [i]. The RDSM samples the input signal for *M* times and the sampled input signal is accumulated in the integrator while the output of the integrator is negatively fed back to the input with a one-bit ADC and one-bit DAC. The factor of 1/2 in front of the integrator is used for reducing the maximum amplitude of the integrator to be equal to the input signal range [ii, v]. The number of 1's of the one-bit ADC output is counted with the *m* (=$\log_2$M)-bit counter for generating an *m*-bit coarse digital code. The extended ADC used for the integrator output is assumed to be converted to an n-bit fine digital code. The final output is the sum of the counter and the extended ADC outputs. The resulting resolution of the entire ADC is *m+n-1* bits by considering the code redundancy necessary for avoiding the non-linearity error due to the threshold-level variation of the one-bit ADC[i, ii].

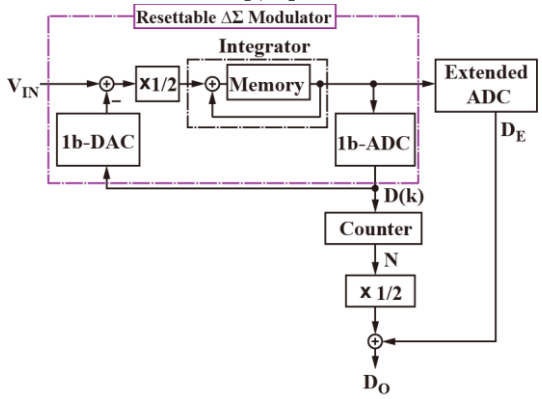

Fig. 1. Block diagram of the multiple-sampling based ADC.

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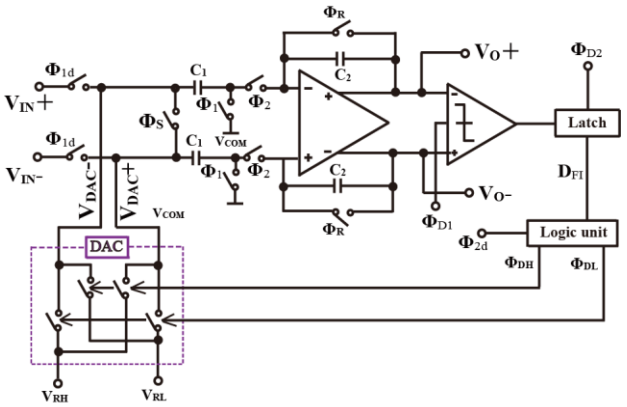

Fig. 2. Schematic diagram of the RDS ADC.

2.2 Circuits and operation of the RDSM

A schematic diagram of the RDSM is shown in Fig. 2. It consists of a switch-capacitor integrator with a fully differential operational amplifier, one-bit sub-ADC, logic unit and one-bit digital-to-analog converter (DAC). The one-bit sub-ADC is a comparator with latch (FF) and works for comparing the integrator output with zero. The logic unit performs the logical function which controls the DAC operation. The single-ended equivalent circuit and operation phase diagram of the RDSM is shown in Fig. 3(a) and Fig. 3 (b), (c) and (d), respectively. It works with three phases of reset (Fig. 3(b)), sampling (Fig. 3(c)) and charge transfer (Fig. 3(d)). In the reset phase shown in Fig. 3(b), the switch controlled by Φ_R is turned on and the charge in the feedback capacitor C_2 is reset. In the sampling phase shown in Fig. 3(c), the switches controlled by Φ_{1d} and Φ_1 are turned on and the input signal is sampled in the capacitor C_1. The switches by Φ_{1d} and Φ_1 are activated at the same time but the switch by Φ_1 is turned off first for bottom plate sampling to reduce the signal-dependent charge injection of switches. In the charge transfer phase (Fig. 3(d)), the switches Φ_{1d} and Φ_1 are turned off and the switch by Φ_2 is turned on and the charge in C_1 is transferred to C_2. In this phase, the input terminal of C_1 is connected to the one-bit DAC, and the charge transferred from C_1 to C_2 is proportional to the difference between the input signal and DAC output. The ratio of C_1 to C_2 is set to 1/2 for setting the gain factor in front of the integrator to be 1/2, i. e., $C_2=2C_1$. The comparator as the one-bit ADC is operated with the clock Φ_{D1} in the input sampling phase and the output of the comparator is operated with the clock Φ_{D2}. The latched output is used for logical operation with the clock Φ_{2d}, to generate the clocks Φ_{DH} and Φ_{DL} which are used for controlling the one-bit DAC and the difference of the two analog reference levels V_{RH} and V_{RL} are generated as the DAC output. The sampling phase and charge transfer phase are repeated for *M* times and the gain of the integrator to the input after *M*-time sampling equals to *M*/2 considering the gain factor of 1/2 in front of the integrator. This gain due to the multiple sampled integration has a great effect of the input-referred thermal noise reduction and the folding operation using the one-bit sub-ADC and one-bit DAC leads to high dynamic range of the input signal.

The fundamental equation of the operation of the RDSM for each cycle (the *i*-th cycle, *i*>2) if this ADC is operated without any errors is expressed as

$$V_O(i) = V_O(i-1) + 0.5\{V_{IN}(i) - V_{DAC}(i)\} \quad (1)$$

where $V_{IN}(i)$, $V_O(i)$ and $V_{DAC}(i)$ are the input signal, output signal of the integrator and DAC output signal, respectively at the *i*-th cycle. In the fully differential type of implementation as shown in Fig. 2, $V_{IN}(i)$, $V_O(i)$ and $V_{DAC}(i)$ are given by

$$V_{IN}(i) = V_{IN}^{+}(i) - V_{IN}^{-}(i) \quad (2)$$

$$V_O(i) = V_O^{+}(i) - V_O^{-}(i) \quad (3)$$

$$V_{DAC}(i) = \begin{cases} V_R & (V_O(i-1) \geq 0) \\ -V_R & (V_O(i-1) < 0) \end{cases} \quad (4)$$

where $V_{IN}^{+}(i)$ and $V_{IN}^{-}(i)$ are the positive and negative input signals at the *i*-th cycle, respectively, $V_O^{+}(i)$ and $V_O^{-}(i)$ are the positive and negative output signals of the integrator at the *i*-th cycle, respectively, and V_R is given by $V_R=V_{RH}-V_{RL}$. In the first two cycles, the DAC is not operated and the input signal is sampled C_1 and transferred to C_2 by turning the switch controlled by Φ_S on. Then the outputs of the first two cycles are given by $V_O(1) = 0.5V_{IN}(1)$ and $V_O(2) = 0.5(V_{IN}(2)+V_{IN}(1))$ if the initial output of the integrator is assumed to be zero, i. e., $V_o(0) = 0$.

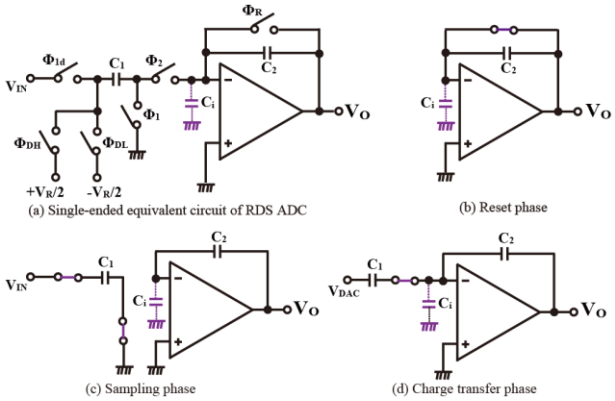

Fig. 3. Circuit operation of the RDSM.

In the implementation of the RSDM, analog imperfection of the circuits causes errors in the fundamental equation of Eq. (1) and worsens the linearity. The analog imperfection may include a finite gain of the operational amplifier (op-amp), capacitor mismatch between C_1 and C_2, charge injection of switches, incomplete settling of the integrator, offset of the op-amp and offset of the comparator. The charge injection with bottom-plate sampling and op-amp offset do not influence to the linearity. The RSDM has a tolerance in linearity to the comparator offset if the offset is relatively small [i]. An incomplete settling error is another important error component in high-speed low-power design of the ADC, but it is assumed to be small enough here. The fundamental equation in each cycle considering the error components due to capacitor mismatch and finite op-amp gain can be derived using charge conservation law at the charge summation node as

$$(1+e_{fg})V_O(i) = (1+e_{fg2})V_O(i-1) + 0.5(1+e_m)\{V_{in}(i) - V_{DAC}(i)\} \quad (5)$$

where e_{fg}, e_{fg2} and e_m are terms due to errors and are given by

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$$e_{fg} = \frac{C_1 + C_2 + C_i}{C_2 G_A},\quad e_{fg2} = \frac{C_2 + C_i}{C_2 G_A} \text{ and } e_m = 2\frac{C_1}{C_2} - 1 \quad (6)$$

and where C_1 and C_2 are capacitances of C_1 and C_2 with mismatch deviations, respectively, C_i is the parasitic capacitance at the input terminal of the op-amp and G_A is the open-loop DC gain of the op-amp. The ideal capacitance ratio of C_1 to C_2 is 0.5. Equation (5) is re-written as

$$V_O(i) \cong (1+e_1)V_O(i-1) + 0.5(1+e_2)\{V_{in}(i) - V_{DAC}(i)\} \quad (7)$$

where, e_1 and e_2 are $e_1 = (e_{fg2} - e_{fg})/(1+e_{fg}) \cong e_{fg2} - e_{fg}$ and $e_2 = (e_m - e_{fg})/(1+e_{fg}) \cong e_m - e_{fg}$, respectively.

2.3 Overall Error of the RDSM

In order to build an error correction model for the RDSM in digital domain, the Eq. (1) is writen as

$$Y(i) = Y(i-1) + 0.5\{X(i) - D(i)\} \quad (8)$$

where

$Y(i) = V_0(i)/V_R$,

$X(i) = V_{IN}(i)/V_R$ and $D(i) = V_{DAC}(i)/V_R$.

After *M*-time sampling and integration, the equation for the RDSM can be expressed as

$$Y(M) = 0.5\left\{\sum_{i=1}^{M} X(i) - \sum_{i=3}^{M} D(i)\right\} \quad (9)$$

if *Y(0)* is set to 0. In the RSDM, the input signal during the operation is assumed to be a DC level. To derive the formula for the digital error correction for the static non-linearity improvement, it is assumed that the *M* samples of the input take their mean value $\overline{X}$, i.e., $X(1) = X(2) = \cdots = X(M) = \overline{X}$. Then Eq. (9) is expressed as

$$0.5M\overline{X} = Y(M) + 0.5N \quad (10)$$

where $N = \sum_{i=3}^{M} D(i)$ is the counter output code. Equation (10) means that the final digital output which is the digitized input amplified by the gain of 0.5*M* is given by the sum of the counter output code and Y(M) which is digitized by an extended ADC as shown in Fig. 1. If the extended ADC output is denoted by D_E, the final digital output is given by $D_E + 0.5N$. Similar to Eq. (8), Eq. (7) is expressed as

$$Y(i) = (1+e_1)Y(i-1) + 0.5(1+e_2)\{X(i) - D(i)\} \quad (11)$$

where $Y(i)$ and $D(i)$ are $V_0(i)/V_R$ and $V_{DAC}(i)/V_R$, respectively, for the case that the RDSM has errors. After *M*-time sampling and integration, the final output $Y(M)$ if $Y(0)$ is zero and the first two cycles are operated without the DAC is expressed as

$$Y(M) = 0.5(1+e_2)\left\{\sum_{i=1}^{M}(1+e_1)^{M-i}X(i) - \sum_{i=3}^{M}(1+e_1)^{M-i}D(i)\right\}. \quad (12)$$

If *M* samples of the input take their mean value $\overline{X}$, Eq. (12) is expressed as

$$Y(M) = 0.5(1+e_2)\left\{\overline{X}\sum_{i=1}^{M}(1+e_1)^{i} - \sum_{i=3}^{M}(1+e_1)^{M-i}D(i)\right\} \quad (13)$$

III. DIGITAL ERROR CORRECTION OF THE RDSM

Equation (13) is approximated to

$$Y(M) \cong 0.5(1+e_2+e_1\frac{M-1}{2})M\overline{X} - 0.5N(1+e_2) - 0.5e_1\sum_{i=3}^{M}(M-i)D(i) \quad (14)$$

if the second or higher order error terms such as e_1e_2 and e_1^2 are ignored and where $N = \sum_{i=3}^{M} D(i)$. It is also expressed as

$$0.5(1+E_G)M\overline{X} \cong Y(M) + 0.5N - E_1 - E_2 \quad (15)$$

where $$E_G = e_2 + \frac{M-1}{2}e_1 \quad (16)$$

is the overall gain error, and

$$E_1 = -0.5e_1\sum_{i=3}^{M}(M-i)D(i) \quad (17)$$

and

$$E_2 = -0.5e_2N \quad (18)$$

are error terms on nonlinearity due to e_1 and e_2, respectively. Eq. (15) means that the error in the digitized input amplified by the gain of *M* can be corrected by subtracting error terms of E_1 and E_2 at the ADC output. Since E_G does not influence to the non-linearity of the ADC, the error is not corrected if the accuracy of the gain is not a concern.

The measurement for error coefficients can be done by using the integral non-linearity measurement of the ADC. To determine the optimized value of e_1 and e_2 for better linearity of the ADC, the cost function calculated from the mean square of the integral nonlinearity can be used. The cost function is given by

$$\eta = \frac{1}{N}\sum_{i=1}^{N} INL_i^2 \quad (19)$$

where INL_i is the integral nonlinearity of the *i*-th ADC code. Using this cost as a function of e_1 and e_2, the error coefficients to minimize the nonlinearity error of the ADC are obtained by searching the minimum of the cost function. In order to approach to the optimum values of e_1 and e_2, with fewer number of measurements of η, a technique similar to that described in ref. [ix] can be used.

IV. SIMULATION RESULTS

In order to confirm the validity of the proposed digital error correction technique for the RDSM, an ADC shown in Fig. 2 is designed using the parameters in 65nm CMOS technology and the digital error correction is applied to the data obtained by circuit simulations. The simulated transfer curves of the RDSM for *M*=16 is shown in Fig. 4. The power supply voltage is 1.2V, the clock frequency is 10MHz, and V_{RH} and V_{RL} are 0.9V and 0.3V, respectively. The input signal range is set to -0.6V to 0.6V. The integrator output is folded 14 times as shown in Fig. 4(a). The counter counts the number of folds and the counter output is incremented as the input signal

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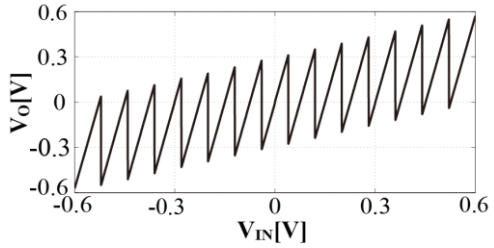
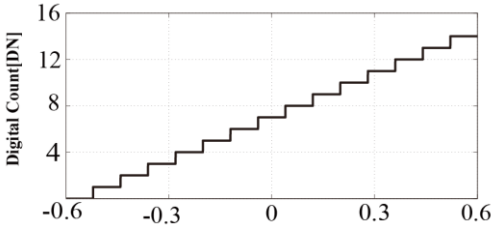
increases as shown in Fig. 4(b). To demonstrate that the digital error correction is effective even for the ADC with large errors due to analog imperfection, the ADC is designed using a folded-cascade type op-amp with relatively small open-loop DC gain of 49.4dB and small sampling capacitance of 100fF as C_1. With this small capacitance, large capacitance mismatch of -0.50% is assumed [x, xi].

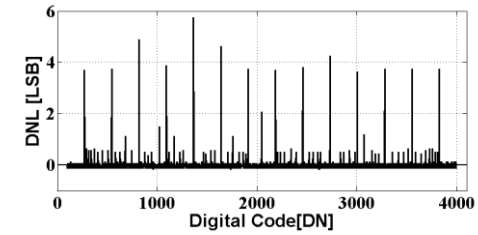


(a) Transfer curve of the analog output.

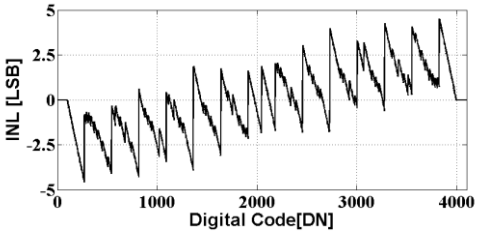


(b) Counter output

Fig. 4. Simulated transfer curve of the designed ADC.



(a)



(b)

Fig. 5. Simulated non-linearity plots for the 12-bit RDSM before calibration. (a) DNL (b) INL.

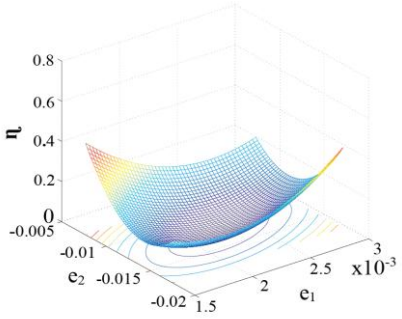
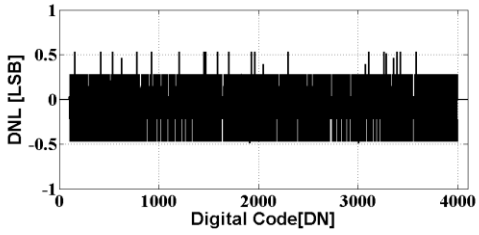
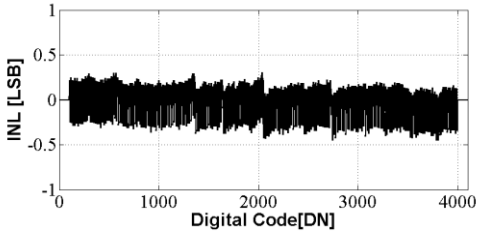


Fig. 6. Cost as a function of two error components.



(a)



(b)

Fig. 7. Simulated non-linearity plots for the 12-bit RDSM after calibration with optimized value of error coefficients. (a) DNL (b) INL.

The differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC before error correction is shown in Fig. 5. These linearity data are obtained by the counter output as a coarse ADC code (Fig. 4(b)) and the analog output shown in Fig. 4(a) which is assumed to be digitized by an ideal 11-bit ADC. The DNL and INL are evaluated at 12-bit resolution and the horizontal axis of Fig. 5 is expressed as 12-bit code range. The maximum DNL and INL at 12bits before error correction are +5.75/-0.18[LSB_{12}] and +4.52/-4.58[LSB_{12}], respectively, where LSB_{12} is one LSB at 12-bit resolution.

Because of the influence of many different analog imperfections, the best coefficients to minimize the non-linearity errors estimated by the optimization using the cost function calculated with the INL curve given by Eq. (19). Figure 6 shows a plot of the cost by the INL of the designed ADC with error corrections as a function of the applied error coefficients of e_1 and e_2. The minimum of the cost function is found at e_1 and e_2 of 0.22% and -1.25%, respectively, which are close to the error coefficients with theoretical equations of Eq. (6) considering capacitor mismatch and finite gain error only. The DNL and INL plots after the error correction using these coefficients are shown in Fig. 7(a) and Fig. 7(b), respectively. The maximum DNL and INL are reduced to +0.53/-0.49 [LSB_{12}] and +0.30/-0.45[LSB_{12}] respectively.

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Table I. Maximum DNL and INL for different resolution on the extended ADC.

No. of bits in extended ADC	11-bit	12-bit	13-bit
DNL	+0.53/-0.49	+0.28/-0.29	+0.16/-0.26
INL	+0.30/-0.45	+0.18/-0.33	+0.12/-0.24

The effectiveness of the digital error correction to the RDSM depends on the resolution of the extended ADC. The DNL and INL data shown in Fig. 5 and 7 are obtained by using ideal 11-bit ADC. The Table I shows the maximum DNL and INL for different resolutions on the extended ADC. The real implementation of the ADC should use a lower-resolution extended ADC for the cost effectiveness. In this sense, the 11-bit extended ADC is good enough for realizing true 12-bit resolution in the entire ADC, though a higher linearity is expected by using higher resolution in the extended ADC.

A possible problem of the influence of the nonlinearity of the extended ADC to that of the entire ADC is not discussed here. This is because the problem of nonlinearity in the extended ADC is relaxed by the gain of the RDSM. For instance, in the RDSM with *M* of 16, the gain of 8 is applied to the signal before the extended A/D conversion. Because of this, the requirement of linearity in the extended ADC is 9-bit level for the entire ADC of 12bits. Even if the nonlinearity of the extended ADC is needed to be corrected, it can be corrected by conventional techniques. For instance, if the extended ADC is implemented with a cyclic ADC, a technique of digital error correction proposed in ref. [ix] can be used.

V. CONCLUSION

This paper has presented a digital error correction technique for the multiple-sampling based ADC which uses a resettable delta-sigma modulator (RDSM) with a counter for coarse conversion and extended ADC for fine conversion. The RDSM dominates the entire linearity of the ADC and the non-linearity of the RDSM due to the capacitor mismatch and finite op-amp gain is corrected in digital domain. The RDSM is designed with 65nm CMOS technology and the circuit simulation results are used for the demonstration of the effectiveness of the digital error correction technique. The DNL and INL at 12-bit resolution are improved from +5.75/-0.18 LSB to +0.53/-0.49 LSB and +4.52/-4.58 LSB to +0.30/-0.45 LSB, respectively, using the optimized error coefficients based on the proposed non-linearity error model of the RSDM.

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