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A New-High Speed-Low Power-Carry Select adder Using Modified GDI Technique

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Abstract: Adders are of fundamental importance in a wide variety of digital systems.This paper presents a novel bit block structure which computes propagate signals as carry strength. Power consumption is one of the most significant parameters of carry select adder.The proposed method aims on GDI(Gate Diffusion Input) Technique.Modified GDI is a novel technique for low power digital circuits design further to reduce the swing degradation problem.This techniques allows reduction in power consumption,carry propagation delay and transistor count of the carry select adder.This technique can be used to reduce the number of transistors compared to conventional CSLA and made comparison with known conventional adders which gives that the usage of carry-strength signals allows high-speed adders to be realised at lower cost as well as consuming lower power than previous designs.Hence,the proposed architecture mainly concentrating on the area level & reducing the power using modified GDI logic.

Keywords-- Fast Adder,Modified GDI,Low power design.

I. INTRODUCTION

Low power arithmetic circuits have become very important in VLSI industry.Due to the rapid growth of portable electronic component,Adder circuit is the main building block in DSP processor. Adder is the main component of arithmetic unit. A Complex DSP system involves several adders.The Designers are forced with more constraints are high speed , high throughput , small silicon area and low power consumption.Many design styles of adders exist.Although,Ripple carry adders are the small in design structure but its very slower. Most recently, carry-skip adders [1, 2, 3] are used popularly due to their performance of high speed and small size. Generally, in an N-bit carry-skip adder divided into M-bit number of blocks [1, 4], a long-range of carry signal starts at a block Bi, which rippling through some bits in that block, then it skips some blocks, and ends with a block Bj. Carry-look-ahead and carry-select adders are very fast but far larger and consume much more power than ripple or carry-skip adders. Two of the fastest known addition circuits are the Lynch-Swartzlander's [5] and Kantabutra's [6]hybrid carry-look-ahead adders. They are based on the usage of a carry tree that produces carries intoappropriate bit positions without back propagation. In order to obtain the valid sum bits as soon as possible, in both Lynch-Swartzlander's and Kantabutra's adders the sum bits are computed by means of carry-select blocks, which are able to perform their operations in parallel with the carry-tree.

This paper presents two new families of adders, both based on a new bit carry Select & adiabatic structure that computes propagate signals called "carry-strength" in a ripple fashion.

The first family of adders is a family of new carry-select adders that are significantly faster than traditional carry-select adders while not much larger. The second family of adders is a family of hybrid lookahead adders similar to those presented in [5, 6] but significantly smaller and still comparable in speed. Carry Select Adder(CSLA) is one of the fastest adder used in many data-processing processors to perform fast arithmetic functions.This work uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. There is scope to reduce the power consumption in the regular CSLA. Multiple pairs of Ripple Cary Adders (RCA) are used in CSLA structure. Hence, the CSLA is not area efficient. We proposed a modified CSLA design. This paper presents new families of adders, both based on a new bit carry Select & adiabatic structure that computes propagate signals called "carry-strength" in a ripple fashion. The family of adders is a family of new carry-select adders that are significantly faster than traditional carry-select adders while not much larger.

Multiple pairs of Ripple Cary Adders (RCA) are used in CSLA structure. Hence, the CSLA is not area efficient. CSLA generates many carriers and partial sum.Many architecture is tested under different conditions which possibly result in variant performance even implemented with the same algorithm,CSLA is proved to have good performance using in high speed adder. CLA is proved to have good performance which is using in high speed adder.Since, this architecture are used commonly in many papers. STCLA – Spanning Tree Using CLA uses a tree of 4-bit Manchester Carry-Lookahead chains (MCC) to generate carry for different bit position. RCLCSA – Recursive CLA/CSA Adder uses the same conception as STCLA except the lengths of its carry chains are variant, not fixed. HSAC – High Speed Adder Using CLA uses Ling's adder which solves the transition of carry propagation delay.

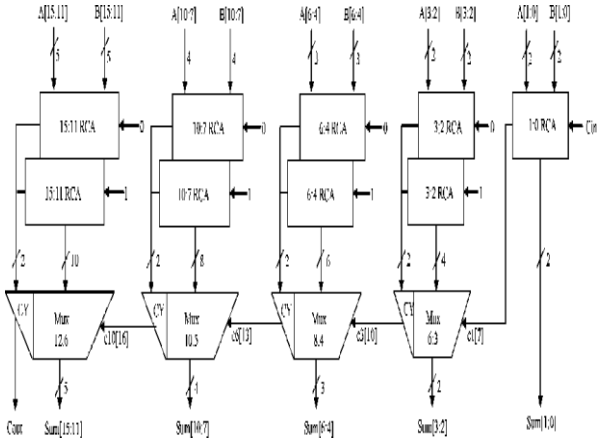

Figure 1. Conventional Carry Select Adder using RCA

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Adders using different implementation that is the most critical one. For example, STCLA and RCLCSA uses dynamic CMOS design while HSAC using static CMOS. A general architecture is to implement for measuring this three different algorithm that means we can use both dynamic CMOS as well as the static CMOS to implement these algorithms for comparison. A New architecture improved from the original paper.Original implementation which is based on the Adiabatic logic,but it takes more advantage on the characteristics of CMOS circuit. Generally, we don't use "bar"(inverted) as we conduct every equation . But in reality, "bar" is added at the output of logic circuits automatically. So, they use this special characteristic to reduce the carry propagation time. Gate Diffusion Input (GDI) is an advanced technique for low power digital design .This technique can be used to reduce power consumption, delay and number of transistors compared to Conventional CMOS design.The standard CMOS and several different techniques for circuit design is compared with Modified GDI technique.

II. PROPOSED GDI BASED CSLA ARCHITECTURE

Basic GDI Cell : The Basic GDI design [5] is as shown in Fig. 2, which can be implemented using twin-well CMOS or SOI technology. Basic GDI cell consists of 3 input terminals G, P and N.From Figure 2, source and drain connected with P and N terminal.

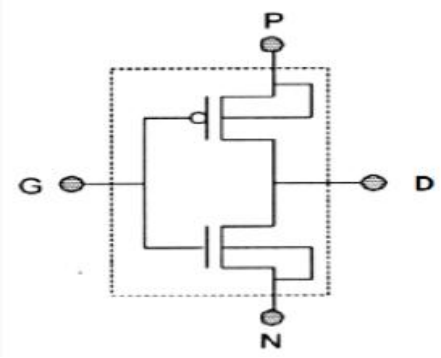

Figure 2.Basic GDI Cell

Power dissipation becomes most important limitation in high performance applications. Optimizations of Basic logic gates are fundamental constraint in order to get better the performance of [6] a variety of low power and high performance devices.A high-speed logic style for low power electronics design is known as Gate Diffusion Input (GDI) with less power dissipation, less design area, and efficient implementation of huge variety of logic functions. But this basic Gate Diffusion Input (GDI) logic style suffers from some of the practical limitations like swing degradation, fabrication complexity and bulk connections. These limitations can be overcomes by modified gate diffusion input (Mod-GDI) logic[5].This modified gate diffusion input (Mod-GDI) logic allows reduction in power consumption, delay and area of digital circuits. Figure 3 shows that the basic Mod-GDI cell.

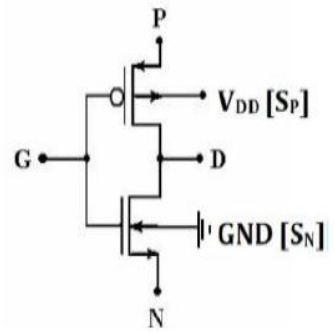

Figure 3. Modified GDI Cell

Comparison made with basic GDI cell, Modified GDI cell contains,

i. a low voltage terminal (SP) configured to be connected to supply voltage
ii. a high voltage terminal (SN) configured to be connected to ground.

Including terminals,we can ensures that the Mod-GDI cell can be implemented with all current CMOS technologies.In Mod-GDI cell, the bulk node of all PMOS transistors are connected to VDD and bulk node of all NMOS transistors are connected to GND. Mod-GDI cell uses standard 4 terminal NMOS and PMOS transistors and it provides ease of implementation in all type of standard CMOS technology. Table 1 represents [8] the various logic functions which can be implemented with help of MOD-GDI cell for different input configuration. This arrangement of modified GDI cell provides reduction in both sub -threshold and leakage power [17] compared to static CMOS gate. Mod-GDI is more suitable while designing of high speed, low power circuits by using reduced number of transistors as well as improved swing degradation and static power characteristics.This logic allows simple top-down design by using a small cell library [8]. Mod - GDI logic performance is testable, so that Mod-GDI logic and logic circuit design methods is hopeful for design a low power and high performance applications.

In Figure.1, Logic gates can be replaced by Mod-GDI cell to achieve high speed efficient carry select adder with low power consumption and less layout area.Each logic gates in conventional CSLA based on RCA is replaced by modified GDI logic cells.Performance comparison also done with conventional CSLA and Mod-GDI based CSLA.

III. OBSERVARTIONS

A. TABLE-I

Various logic function implementation with Mod-GDI logic:

S_N	S_P	G	P	N	D	FUNCTION
0	1	A	1	0	A'	INVERTER
A	A	B	0	A	AB	AND
0	D	B	A	1	A+B	OR
0	A	B	A	A'	A'B+AB'	XOR
0	A	B	A'	A	AB+A'B'	XNOR
0	1	A	B	C	A'B+AC	MUX

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B. POWER & DELAY CALCULATION

(1) Power consumption obtained for Conventional 16 bit CSLA based RCA architecture:

i. Vdd Gnd from time 0 to 1e-006
ii. Average power consumed -> 8.851721e-002 watts
iii. Max power 6.643323e-001 at time 4.02938e-007
iv. Min power 1.448529e-001 at time 3.11e-007

(2) Delay obtained for Conventional 16 bit CSLA based RCA architecture:

→ TRAN_Measure_Delay_1 = 5.2892e-008

C. (1)Power obtained for Proposed Mod-GDI based 16 bit CSLA architecture:

i. Vdd Gnd from time 0 to 1e-006
ii. Average power consumed -> 4.543197e-003 watts
iii. Max power 5.686588e-002 at time 4.00756e-007
iv. Min power 9.378497e-008 at time 4.2e-007

(2)Delay obtained for Proposed Mod-GDI based 16 bit CSLA architecture:

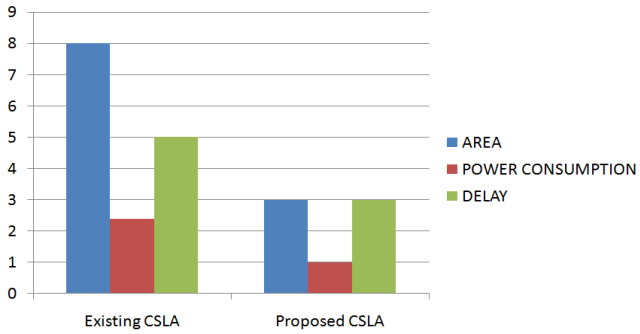
→ TRAN_Measure_Delay_1 = 4.7000e-009 .

D. **TABLE-II**

Performance Analysis Table For 16bit-Carry Select Adder:

S.NO	TYPE	AREA	POWER CONSUMPTION	DELAY
1.	Existing CSLA	864T	8.87Mw	52.8ns
2.	Proposed CSLA	352T	0.445mW	4.7ns

E. Performance analysis chart for 16bit-carry select Adder:



From TABLE-II,Performance Comparison made with the conventional 16bit-CSLA and MOD-GDI based 16bit-CSLA.The significant parameter of low power vlsi design such as area,power consumption as well as the delay can be highly reduced by using Mod-GDI logic in Carry Select Adder architecture.

IV. CONCLUSION

The new implementation is based on the original architecture, so it can be used in both static CMOS and dynamic CMOS circuits. And through my proposed architecture, I can reduce power,area consumption but sacrifice some timing (which can be neglected).By this implementation,the proposed Mod-GDI based 16bit-CSLA will prove that is really better than the Conventional CSLA based RCA. From the previous known CSLA architecture, realized that improving the performance of adder is very difficult now because of the transistor level. If to get higher performance we must reduce the complexity in transistor level,it can be achieved by GDI logic.But the basic GDI logic suffers from swing degradation problem and flexibility,so that the Mod-GDI logic can be presented in this paper.Hence,the proposed carry select adder architecture ensures that the less power consumption and reduced no. of transistors with neglecting of delays

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