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Delay and Power Consumption of Fault Tolerant Data Busses in VDSM Technology

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Abstract- In Very Deep-submicron (VDSM) systems, the scaling of ULSI ICs has increased the sensitivity of CMOS technology to cause various noise mechanisms such as power supply noise, crosstalk noise, leakage noise, etc. In VDSM technology distance between the data bus lines is reduced, so coupling capacitance is dominating factor. Unfortunately, in VDSM systems, the coupling capacitance is of magnitude several times larger than the loading capacitance. The coupling capacitance causes logical malfunction, delay faults, and power consumption on long on-chip data buses .An important effect of the coupling capacitance is Cross talk. Crosstalk is mainly dependent on several factors: drive strength, wire length/spacing, edge rate and propagation duration. The crosstalk noise produces from the coupling capacitance. Such faults may affect data on data bus. To avoid this condition and to guarantee signal integrity on the on-chip communication, a fault tolerant bus can be adopted. This could be achieved by implementing error-correcting codes (ECCs), providing on-line correction and do not require data retransmission. The 4,8,16,and 32-bit data bus is implemented in 180nm, 120nm,and 65nm technologies using Bsim4 model. For reliable transmission of the data ECC techniques is placed on the data bus. We employed a Hamming code and Dual rail as ECC for 4,8,16 and 32-bit fault tolerant data bus. This is implemented in 180nm, 120nm and 65nm technology.

Keywords: coupling capacitance, load capacitance, crosstalk, Hamming code, VDSM, power dissipation.

I.INTRODUCTION

As technology scale down to very deep submicron (*VDSM*) technology, the designers are to face many challenges like power dissipation, delay and various noises. In fact, the reduced feature sizes, reduced node capacitances, increased integration Density , increase in operating frequencies, power supply and noise margins, as well as the process parameter variations make ICs more sensitive and prone to transient faults, crosstalk noise and delay variations. Crosstalk is one of the most important noises that affects long interconnects and global interconnects. Crosstalk on data bus paths is becoming

one of the major concerns for SoC systems. In current trends in integrated-circuit design, it is impossible to eliminate errors caused by crosstalk because of stringent area and performance requirements in recent designs. These noises due to crosstalk could be eliminated by resizing drivers, shielding interconnect techniques, rerouting signals, and repeater insertion techniques. However, these redesign techniques using the analysis of crosstalk-induced noise may be very expensive in terms of time and design efforts [9].

The use of deep sub-micron (DSM) technology in SoCs increases the capacitive coupling between adjacent wires leading to severe crosstalk noise, which causes the functionality or performance of the chip to deviate significantly from expected behavior. Several physical design [14] and analysis [5] techniques have been developed to allow design for margin and to minimize signal integrity problems In VDSM technology, the lumped model for data bus is not accurate to compute the power consumption on the bus during system's normal activity, because this model does not take into account any mutual effect between adjacent wires. An accurate model, which does take mutual capacitances into account, is reported in [1]. This model is shown in Figure 1, where CB (F/m2) is the contribution of the wire to the bottom parallel plate, CEB (F/m) is the contribution of the wire edge to the bottom (the fringing field) and CEC (F/m) is the wire to wire lateral component. In this model the CEC, also called coupling capacitance, dominates and is several times higher than other capacitances. This coupling capacitance causes the crosstalk which introduces the errors on the data buses. Wires paths of data bus are longer and closer one another, and consequently the mutual coupling capacitance or inter wire capacitance is increasing compared with previous technologies. Current and future SoCs will be dominated by a large number of very long interconnects and buses needed for the integration and communication among the cores in the chip. As a consequence, crosstalk effects are getting more and more relevant, and are becoming the main cause of noise and delay uncertainty within a data bus. Crosstalk errors result from parasitic coupling between adjacent bus paths since this coupling injects extra ac current into a coupled path. Crosstalk error can be classified into two types: Crosstalk-induced delays and crosstalk induced glitches. A crosstalk-induced delay [10] occurs when noise is injected on a path when a signal transitions and results in a change in the delay of the path.

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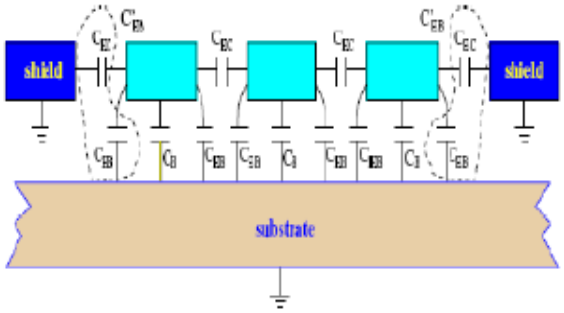

Fig1. Parasitic capacitances of a 3 wire bus above substrate.

II. Crosstalk

Crosstalk induced glitch [13] occurs when a victim line is intended to be at a stable state and results in an unwanted noise pulse on the path. In most circuits, crosstalk-induced delay, particularly slowdown delay, leads to the chip failure more so than the crosstalk-induced glitch [12], [10].

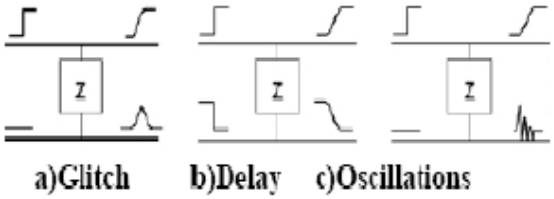

Fig 2: Types of Crosstalk errors.

Increased coupling capacitance between a pair of bus paths can produce either glitches or delays depending upon the signal transitions on the data bus as shown in Fig. 2(a) and (b) respectively. In addition to glitches and delays, presence of significant coupling inductance can result in damped voltage oscillations superimposed on top of a glitch or delay, as illustrated in Fig. 2(c). To satisfy the delay constraints and guarantee signal integrity, several techniques have been proposed, aimed at masked by data retransmission to achieve fault tolerance. Besides these approaches, either error detecting codes reducing the crosstalk-induced delay uncertainty. The most common practices are: i) to insert repeaters [6,2] and ii) to shield the wires[11]. Furthermore, it has been recently shown that, by introducing an intentional delay among coupled signal transitions, the crosstalk due delay can be reduced [3]. For on-chip global interconnections, the reliability issue can be addressed by implementing techniques based on on-line testing and diagnosis, followed by proper fault recovery. For instance, an error due to noise affecting the bus wires can be first concurrently revealed using a specific detector and then followed by proper recovery, or error correcting codes, which provide on-line correction and do not require retransmission can be implemented. The adoption of coding techniques implies the use of an encoder that, starting from the information bits, calculates the check bits. These generated check bits are, therefore, delayed with respect to the information bits by a time interval equal to the delay introduced by the encoder.

III. GENERAL BLOCK DIAGRAM DESCRIPTION FOR FAULT TOLERANT DATA BUS

General correction scheme for a fault tolerant bus is shown in Fig-3. The k information its (d0,…..dk-1) are given to the inputs of an encoder (E), which produces m check bits (c0,…cm-1).These n= k+m bits are transmitted on the bus and form a codeword belonging to a code space with minimum hamming distance dmin (i.e., the no. of differing bit positions) that is required to achieve the desired degree of error correction (e.g.,dmin=3 for single error correction). At the receiver end of the bus, the decoder (D) detects and corrects the possible errors which might have occurred on the busses consists of a Syndrome generator (SG) and a Syndrome detector(SD) directly connected. SG recomputed the parity bits from the received data (d'0……,d'k-1) and compares them with those transmitted on the bus, thus generating an m-bit vector S=(s0,…sm-1), called the error syndrome. The syndrome one-hot decoder(that is, the decoder which can activated only one output at a time, producing output patterns of the kind0010…0) decodes the error syndrome and generates the k-bit error vector E=(e0,…..,ek-1), which drives the corrector block, If the Syndrome is an all zeros vector, we assume that the operation is error free and the data bits are not modified (also E contains all zeros).otherwise, the error vector E contains a 1 in the position of the erroneous information bit, which is consequently corrected by C, which performs the operation dCi=d1i.ei, for i=0,…,(k-1).[10].

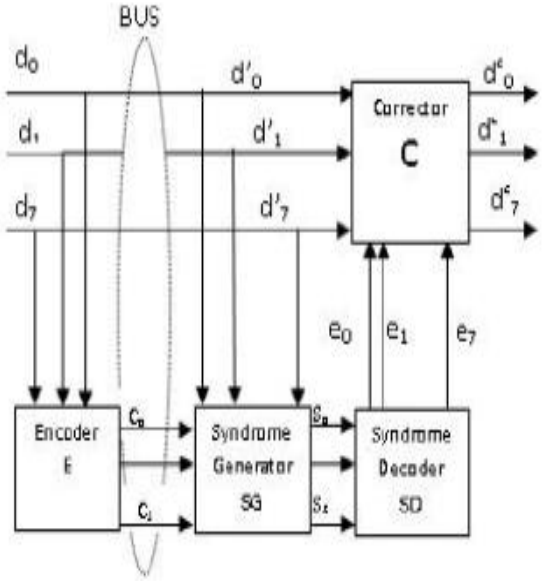

Fig3. Schematic representation of a bus encoding/decoding scheme

IV. ERROR CORRECTING HAMMING CODES

Hamming code is for single bit error detection and correction. In hamming code condition for no. of parity bits required is $2^k \geq m+k+1$

Where k no. of parity bits required

m is no .of message bits

Total no.of bits transmitted in HC is m+k

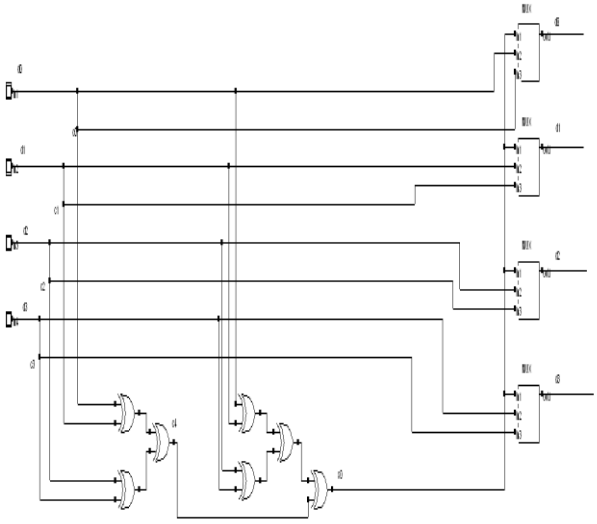

Fig-4: Hardware structure for 8-bit hamming encoding and decoding circuit

V. Error Correcting Dual Rail Code

As for proposed dual rail code, a possible encoding and decoding structure is shown in fig 5.It should noted that only c8 has to be computed, since the check bits c0,…….c7 are a copy of the corresponding data values. Similarly the syndrome pattern consists of only one bit s0, hence no decoding operation is required in order to locate the possible erroneous bit. The correction phase is performed by a set of 2-input multiplexers, each receiving as input a couple (di,ci).These two bits are identical in the error-free case. If an error is present, the signal s0, which acts as a selection bit, allows the correct values to propagate to the output. If no error occurs, or if fault effects one of the check bits c0,……c7,it is S0=0 and the data d0,…..d7 are correctly transferred to the multiplexers' outputs. In the case of error on the data bit, or if a fault affects the bit c8,it is s0=1 and the ECC outputs assume the value of the check bits c0,…..c7,which are correct. Hence the proposed ECC circuit behaves properly.

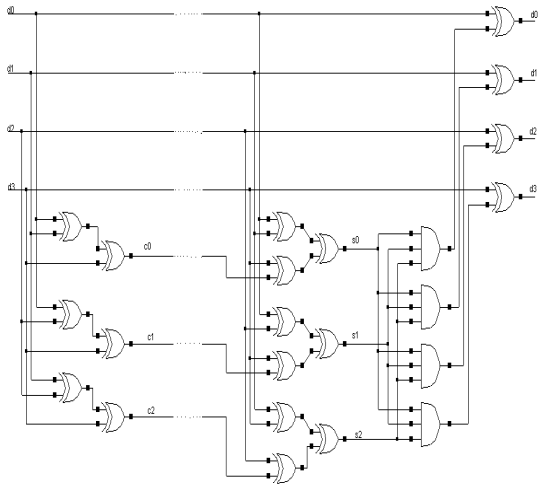

Fig 5: Hardware structure for 8-bit Dual rail encoding-decoding structure

VI. HARDWARE SCHEME AND SIMULATION RESULTS:

Data d0 to d7 is applied to XOR tree based encoder which calculated the check bits (c0 to c3). At the receiving end the check bits are calculated again from the received data. It is compared with the received check bits, in order to compute the syndrome pattern (s0 to s3). The syndrome has then to be decoded in order to determine the position of the erroneous bit, which will consequently be complemented in order to correct it.Fig-5 shows standard encoding and decoding structure for the 8-bit dual rail code. The hard ware structures are implemented in 180nm, 120nm and 65nm technology and its average power, delay are calculated from simulation results. For simulation BSIM4 transistors model is taken into consideration. The simulation results show in below tables

TABLE I AVERAGE POWER (mW)

	180nm	120nm	65nm
Hamming-4 bit	0.737	0.401	0.176
Dual rail -4bit	0.206	0.098	0.0459
Hamming-8 bit	2.135	0.925	0.365
Dual rail -8bit	0.417	0.192	0.0768
Hamming-16 bit	2.288	0.98	0.377
Dual rail -16bit	0.726	0.388	0.156
Hamming-32 bit	3.064	1.164	0.437
Dual rail -32bit	0.926	0.239	0.108

TABLE II DELAY (N-SEC)

	180nm	120nm	65nm
Hamming-4 bit	0.143	0.062	0.077
Dual rail -4bit	0.241	0.112	0.133
Hamming-8 bit	0.385	0.152	0.192
Dual rail -8bit	0.479	0.233	0.262
Hamming-16 bit	0.721	0.274	0.353
Dual rail -16bit	1.026	0.527	0.554
Hamming-32 bit	1.562	0.698	0.796
Dual rail -32bit	2.129	1.235	1.145

VII. CONCLUSION

As the technology moves into nanometer, the effect of crosstalk increases which introduce the errors. For a reliable communication over the data bus a fault tolerant bus using Hamming and Dual rail can be employed at the cost higher power dissipation, delay and area over head. Compare to hamming ECC, Dual rail consumes less power and it contain high delay and average power and delay of hamming and dual rail are decreases as technology scale down.

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